3D ICs-power Analysis Using Cylindrical and Co-axial Through Silicon Via (TSV)

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Abstract: In this study, analytical model and electrical equivalent circuit of Through Silicon Via (TSV) is analyzed. Through silicon Vias form an integral component of the 3-D IC technology by enabling vertical interconnections in 3-D ICs. Among various types, the performances of the simplified lumped TSV model of cylindrical and co-axial type were studied. The performance analyses of these structures were presented by introducing these structures between the tiers of digital circuits. The power consumption of the transistor level digital circuits for single tier without TSV and multiple tiers with cylindrical TSV and Co-axial TSV was simulated using Virtuoso Schematic Editor of Cadence. The comparison for cylindrical and co-axial TSV model with different level tiers were tabulated and performed.

Keywords: Three-dimensional ICs, Through Silicon Via (TSV), TSV lumped RLC model

INTRODUCTION

To increase the functionality and Integration density, the recent advancements in semiconductor processing technologies have enabled three dimensional circuit designs and implementation of heterogeneous systems in the same platform, i.e., Flash, DRAM and SRAM placed on top of logic devices and microprocessor cores (Knickerbocker et al., 2008). 3-D Integration has been considered as the leading technology to overcome the planar IC scaling down limitations such as increased power consumption, wire delay, process variation and cost with the technical node evolution. 3D IC technology helps in mitigating the interconnect problems by reducing the global interconnect wiring length and simultaneously reducing the chip area. Many long interconnects required in 2D chips can be replaced by a 3-D chip by short vertical interconnects. This improves the circuit performance and reduces the total wiring length needs for a system (Van Olmen et al., 2008). Among, Several 3-D integration technologies that have been explored recently, 3D TSV (Through Silicon via) Architecture has proven to be the key enabling Technology.

Through Silicon Via (TSV) is a vertical interconnect element which connects multiple dies and routes the electrical signal and power supply path through all the chips in the stack. TSVs shorten the chip-to-chip interconnects, enable products with higher electrical performance, lower power consumption, wider bandwidth, higher density, smaller form factor, lighter weight and eventually lower cost (Xu and Lu, 2012). The Main applications of TSV are of WLAN, cellular applications and for high performance server and super computer chips. Today there is a variety of TSV structures fabricated and characterized, with various sizes, heights, aspect ratios, materials, densities and processes such as cylindrical TSV, tapered TSV, annular TSV, co-axial TSV, etc. Depending on its structural merits, coaxial through-silicon via (TSV) which has explored recently is a promising 3-D integration solution, which can offer lower coupling with its surrounding environment and achieve better electromagnetic compatibility and signal integrity than other TSV structures (Xu and Lu, 2012). The objective of this study is to analyze the parameters of TSV Model and the performance comparison of Cylindrical and Co-axial TSV RLC Model by introducing these structures between the tiers are verified by using the Virtuoso Schematic Editor. Cadence enables global electronic design innovation and plays an essential role in the creation of today’s integrated circuits and electronics.

MATERIALS AND METHODS

In the 3-D TSV first approach (Van Olmen et al., 2008), TSVs are fabricated after FEOL processing and before BEOL processing and enable the interconnection between the Top Metal of the bottom tier and Metal1 of the top tier is as shown in the cross section of Fig. 1. Electrodynamic principles aid in understanding the impact of physical and technological parameters on $R_{TSV}$, $L_{TSV}$ and $C_{TSV}$.

Cylindrical model: It is the most common TSV scheme where a cylindrical or square conductive metal layer is surrounded by an isolation layer. Due to a thin isolation dielectric (ILD) layer and large extension...
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where, $s_{TSV}$ is the spacing between two TSVs. Spacing between two TSVs varies depending on their location. For example, the mutual coupling between two neighbor TSVs in either vertical or horizontal direction have a space $m$, while two TSVs mutually coupled in diagonal direction have a space $m$:

$$L_i^{VDD} = L_{self}^{VDD} + \sum_{j \text{neighbors}} \alpha_{j} L_{M_{j}}^{VDD} - \sum_{k \text{neighbors}} \alpha_{k} L_{M_{k}}^{GND} \quad (4)$$

$$L_i^{GND} = L_{self}^{GND} + \sum_{j \text{neighbors}} \alpha_{j} L_{M_{j}}^{GND} - \sum_{k \text{neighbors}} \alpha_{k} L_{M_{k}}^{VDD} \quad (5)$$

where, $L_i^{VDD}$ is the inductance for a power TSV and $L_i^{GND}$ is the inductance for ground TSV. Coefficient is the ratio of currents flowing through the TSV under investigation and its neighboring TSV as the current flow on each TSV can differ based on the switching activity of the underlying circuits. For example, a TSV located on the boundary of the TSV array has fewer neighboring TSVs than a TSV located in the center of the TSV array. Hence their mutual inductance would vary. Additionally, mutual inductance varies with respect to the distance between TSVs, as the space between two TSV increases, their coupling decreases as well.

**C_{TSV} model:** TSV capacitance can be derived by solving Poisson’s equations for MOS capacitor structure in cylindrical coordinate system due to TSV shape (Topol et al., 2006).

It is sufficient to solve 1-D Poisson’s equation along radial direction to obtain the capacitance (Katti et al., 2010). Equation (6) describes TSV capacitance as a function of oxide and depletion capacitance as:

$$C_{TSV} = \frac{C_{OX} C_{dep{\min}}}{C_{OX} + C_{dep{\min}}} \quad (6)$$

where,

$$C_{OX} = \frac{2\pi \varepsilon_{OX} L_{TSV}}{\ln \left( \frac{R_{OX}}{R_{metal}} \right)}, \quad C_{dep{\min}} = \frac{2\pi \varepsilon_{a} L_{TSV}}{\ln \left( \frac{R_{max}}{R_{OX}} \right)}$$

where, $\varepsilon_{OX}$, $\varepsilon_{a}$ are permittivity of oxide and silicon, respectively. As shown in (4), $C_{TSV}$ is directly proportional to the length of TSV and inversely proportional to the dielectric thickness of TSV. With increasing frequency up to 20 GHz, for different µm diameter TSV, its capacitance drops off from 30 to 5 fF (Bermond et al., 2009). In this study, we utilize parasitic values obtained for different TSV geometries are listed in Table 1.

### R_{TSV} model:

The analytical expression of the series resistance of the TSV with respect to its radius and per unit length is given by:

$$R_{TSV} = \frac{1}{2\pi \delta \sigma} \left( \frac{1 + 1}{a + b} \right) \quad (7)$$

where, $\delta$ is the skin depth, $\sigma$ is the TSV conductivity are inversely proportional to the radius of the TSV. $a$ and $b$ are radius of inner and the outer surface of the conductor.

### L_{TSV} model:

The series conductance per unit length is given by:

$$L_{TSV} = \frac{\mu_{a}^{\mu_{a}}}{2\pi} \ln \left( \frac{b}{a} \right) \quad (8)$$

### C_{TSV} model:

The TSV capacitance is the series combination of the oxide and depletion capacitance. The capacitance per unit length is given by:

$$C_{TSV} = \frac{2\pi \varepsilon_{OX} \varepsilon_{a}}{\ln \left( \frac{b}{a} \right)} \quad (9)$$

### RESULTS AND DISCUSSION

In the Lumped RLC model of a TSV, the $R_{TSV}$ and $L_{TSV}$ cause the voltage drop along the interconnected...
nodes between Metal1 of the top tier and Top Metal of the bottom tier. CTSV is connected between TSV and ground. LTSV is predominant only for clock frequencies with rise and fall times above 3 GHz. As referred from Katti et al. (2010), the approximate model is obtained by ignoring the inductance which reduces to a simplified \( RC \) model. The impact of RTSV and CTSV on the TSV delay can be analyzed with the help of placing the circuit between the inverters. The circuit consists of an inverter placed on the bottom tier driving an inverter on the top tier through TSV RC model. RTSV would cause a minimal impact on the delay.

A predominant impact of CTSV and a reduced impact of RTSV is analyzed, with inverters in alternate tiers connected by TSVs is simulated using Spectre Simulator. RTSV and CTSV are varied and their impact on delay is verified. The RC model and the RLC model of cylindrical and co-axial TSV between the tiers were designed using Virtuoso Schematic tool and its simulated results are shown below.

The input signal \( V_{in} \) (where \( t_r = t_f = 2 \text{ ns}, T = 30 \text{ ns} \) ) given at one end of the RLC model and the output taken \( V_{out} \) at other end without placing them in between tiers is shown in Fig. 3a. By changing the values of CTSV in RC model, the increase in delay and the voltage drop occurs in its output, than the effect of varying the RTSV is shown in Fig. 3b.
Next, the transient response for both the Cylindrical and Co-axial TSV RLC model between tier levels is also analyzed to determine the impact on delay of the TSV RLC Model in 3D Integration as shown below in Fig. 4. In the analysis, the variations in RTSV values for a given value of CTSV do not change the delay significantly but delay increases significantly with increasing CTSV. Thus, changes in RTSV show minimal impact on the delay, while the impact of CTSV is not negligible. When the number of tier level increases the delay and the voltage drop increases significantly and can be minimized by changing the parameter values of CTSV.

Table 2: Comparison table for power analysis of TSVs

<table>
<thead>
<tr>
<th>No. of tiers</th>
<th>Without TSV model (mW)</th>
<th>With cylindrical TSV (mW)</th>
<th>With Co-axial TSV (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 TIER</td>
<td>0.1310</td>
<td>0.525</td>
<td>0.4078</td>
</tr>
<tr>
<td>3 TIER</td>
<td>0.1358</td>
<td>1.568</td>
<td>1.4257</td>
</tr>
<tr>
<td>4 TIER</td>
<td>0.1408</td>
<td>1.861</td>
<td>1.6734</td>
</tr>
<tr>
<td>5 TIER</td>
<td>0.1462</td>
<td>2.153</td>
<td>1.968</td>
</tr>
</tbody>
</table>

The input signal is taken as Vin (where tr = tf = 2ns, T = 30 ns) and the output is taken at Vout. From Fig. 4a and b the minimum in delay and voltage droop occurs for Co-axial model than that of Cylindrical model. By inserting these RLC model between the tier levels and from Fig. 4c and d the Cylindrical TSV Model has some voltage drop and increase in delay in its output than that of Co-axial TSV Model. Further, increase in (workload) no. of tiers also causes some delay and voltage drop which can be of minimized by changing the parameter values of CTSV gives better results.

The Power analysis by its transient response is based on the electrical performance of a 3-D system. Figure 5 shows the proposed flow model. To understand the implications of power integrity for a 3-D system, we start by investigating a single active tier on a multi-tier system.

CONCLUSION

In this study, Closed-form RLC parameters of TSV was derived from physical parameters and material properties of TSVs and then these electrical parameters of TSV are extracted and the voltage drop is verified using Cadence Virtuoso Schematic. The Power analysis for both cylindrical and co-axial TSV between the circuit RLC model for 2, 3, 4 and 5 tiers were presented in Table 2. Comparing both the structures for different
tiers indicate that the Coaxial TSV Structure have much better crosstalk suppression and power consumption than cylindrical TSV Structure.

REFERENCES


