Research Article

Modified Embedded Switched Inductor Z Source Inverter

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Abstract: A novel modified embedded switched inductor Z-source inverter is proposed by inserting the photovoltaic panels at various locations to improve the output voltage boosting performance. The proposed inverter have the concepts of embedded and switched inductor Z source network to have better features in terms of increased voltage boost inversion ability, continuous input current, reduced voltage stress on the switches/capacitors. Simulations are carried out by employing (120°) pulse width modulation scheme. Hardware implementation of the proposed topology of rating 150 W, 60 V is made and the results are experimentally verified. Switch device power and reliability evaluation of the proposed inverter are also calculated.

Keywords: Embedded network, reliability evaluation, switched inductor network, Z-Source Inverter (ZSI)

INTRODUCTION

Ever increasing energy consumption, cost of fossil fuels, soaring costs and exhaustible nature and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting Sun’s energy directly into electricity. Photovoltaic generated energy can be delivered to power system networks through grid connected inverters. Z source inverters are recent find in inverter topologies mostly used for photovoltaic applications because they have many advantages like better voltage boost and improved reliability than the other traditional voltage and current type inverters (Peng, 2003; Saravanan et al., 2011). Voltage type Z source inverters are classified based on number and location of input dc sources, Z networks and switching devices as reported in (Loh et al., 2010; Li et al., 2013).

Various Z source inverter topologies and its variants are reported in the literature focusing on renewable energy and adjustable speed drive applications (Loh et al., 2005; Saravanan et al., 2012a, b). Various Pulse Width Modulation (PWM) strategies employed in these topologies are discussed in Loh et al. (2005) and Ellabban et al. (2009).

The work reported in this study have the combined features of embedded ZSI (Loh et al., 2010) and Switched inductor Z Source Inverter (SLZSI) (Zhu et al., 2010) to provide better voltage boosting ability with smoother output voltage waveforms at reduced voltage stress on the capacitors. In addition, the proposed inverter avoids the start up inrush current that could destroy the devices and thereby inverter’s reliability is improved.

A two level embedded Z source inverter (Loh et al., 2010) shown in Fig. 1, has dc sources embedded within X shaped LC impedance network. Here, even if one of the sources fails to feed power to the inverter at times of interruptions or fault conditions, continuous operation is possible by feeding power from the other source.

Switched inductor Z Source Inverter (SLZSI) (Zhu et al., 2010) shown in Fig. 2 has high voltage conversion ratios with a very short shoot through state. It consists of four inductors (L1, L2, L3 and L4), two capacitors (C1 and C2) and seven diodes (D1, D2, D3, D4, D5 and D6). The combinations of L1-L2-D1-D3-L3-L4-D5 and L2-L4-D2-D3-L3 act as the switched inductor cells.

Despite this increase in boost inversion, SLZSI has significant drawback namely current drawn from the source is discontinuous in nature. A decoupling capacitor bank at the front end is used to avoid the current discontinuity and protect the source. In addition, SLZSI cannot suppress the startup inrush current resulting in voltage and current spikes which can destroy the devices connected to it.

To overcome these problems, modified embedded switched inductor Z-source inverter topology is proposed in this study which has the concepts of embedded and switched inductor topologies to have better features, like:

- Input current is continuous
- It provides inrush current suppression at start up
- Capacitor stress voltage is reduced
Modified embedded switched inductor Z-source inverter is obtained by inserting split dc sources into the switched-inductor cells. Multiple PV panels now need not be series-connected at one location, but can be divided into isolated strings, hence minimizing series output reduction caused by shading.

The aim of this study is to propose a modified embedded switched inductor Z-source inverter to provide high voltage boost inversion ability, lower voltage stress across the active switching devices, continuous input current and reduced voltage stress on the capacitors. Simulation and experiments are carried out to validate the proposed topology.

**PROPOSED INVERTER TOPOLOGY AND ITS CONTROL SCHEME**

**Topology description:** Figure 3 shows the circuit of proposed modified embedded switched inductor Z-source inverter topology (MESL Z-source inverter). A
The proposed inverter topology is built by inserting dc sources into the X-shaped impedance network. Since the dc sources are connected directly to the impedance network’s inductors, boosted dc current flows through the inverter smoothly. The modified inverter provides a continuous input current without adding an input passive filter and also exhibits a lower voltage stress on the capacitors with improved reliability.

The MESLZSI topology consist of four inductors and two capacitors for each cell, \((L_1, L_2, L_3, L_4)\) and \((C_1, C_2)\) for first cell and \((L_5, L_6, L_7, L_8)\) and \((C_1, C_4)\) for second cell and seven diodes \((D_{in}, D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_{10}, D_{11}, D_{12}, D_{13}, D_{14})\). The combinations of \(L_1-L_2-D_1-D_3-L_4-D_5-D_7\) act as the switched-inductor cells in a single cell.

For the purpose of analysis, operating states of MESLZSI are simplified into shoot through and non shoot through states. In non shoot through states, the proposed inverter has six active states and two zero states in the inverter main circuit. During non shoot through state, in first cell \(D_1, D_4\) and \(D_7\) are ON, whereas \(D_2, D_3, D_5\) and \(D_6\) are OFF. Inductors \((L_1 - L_4)\) and \((L_5 - L_8)\) are connected in series in this state. Capacitors \(C_1\) and \(C_2\) are charged, whereas the inductors \(L_1, L_2, L_3\) and \(L_4\) transfer energy from dc...
Fig. 4: PWM signal generating unit

Fig. 5: Obtained PWM switching signals

voltage sources to the main circuit. The corresponding voltages across $L_1$, $L_2$, $L_3$ and $L_4$ in this state are $V_{L1\_non}$, $V_{L2\_non}$, $V_{L3\_non}$ and $V_{L4\_non}$ respectively. In second cell $D_8$, $D_{11}$ and $D_{14}$ are off, whereas $D_9$, $D_{10}$, $D_{12}$ and $D_{13}$ are off. $(L_5, L_7)$ and $(L_6, L_8)$ are connected in series. Capacitors $C_1$ and $C_2$ are charged, whereas the inductors $L_5$, $L_6$, $L_7$ and $L_8$ transfer energy from the dc voltage sources to the main circuit. The corresponding

In shoot through state:

\[
\begin{align*}
V_{L1} &= V_{C1} + V_{dc} \\
V_{L2} &= V_{C2} + V_{dc} \\
V_{L3} &= V_{C1} \\
V_{L4} &= V_{C2} \\
i_{C1} &= -2I_{L2} \\
i_{in1} &= I_{L3} \cdot i_{in2} = I_{L2} \\
V_{L5} &= V_{C3} + V_{dc} \\
V_{L6} &= V_{C4} + V_{dc} \\
V_{L7} &= V_{C3} \\
V_{L8} &= V_{C4} \\
i_{C3} &= -2I_{L7} \cdot i_{C4} = -2I_{L6}
\end{align*}
\]  

In non shoot through state:

\[
\begin{align*}
v_{L1} + v_{L3} &= V_{dc} - V_{C2} \\
v_{L2} + v_{L4} &= V_{dc} - V_{C1} \\
V_{PN} &= V_{C1} + V_{C2} \\
i_{C1} &= I_{L2} \cdot i_{in1} \\
i_{C3} &= I_{L3} \cdot i_{C4} = I_{L3} \cdot i_{in2} = I_{L4}
\end{align*}
\]  

Control scheme employed: As discussed earlier, any modulation method (Loh et al., 2005; Ellabban et al., 2009) can be adopted to control the proposed MESLZSI. Figure 4 depicts the pictorial representation of 120° mode of conduction of PWM generator. Here the triangular signal is carrier or switching signal of the inverter, whose switching frequency employed ranges from 10-20 kHz. The modulation generator produces a sine wave signal that determines the pulse width and therefore the RMS voltage output of the inverter. For PWM signal generation, it requires both reference and carrier signals that feed into a comparator which creates output signals based on the difference between the signals. Obtained PWM switching signals are shown in Fig. 5. The proposed inverter consist of six switches named as $S_1$, $S_2$, $S_3$, $S_4$, $S_5$, $S_6$ each device conduct for 120° phase shift. Sequence of firing is in the order 61, 12, 23, 34, 45, 56, 61 and the gating signals are shifted from each other by 60°.

Switching device power calculation: The Switching Device Power (SDP) is expressed as the product of
voltage stress and current stress. The total SDP of an inverter system is defined as the aggregate of SDP of all switching devices used in the circuit (Miaosen and Alan, 2007b; Miaosen et al., 2007a). Total SDP is a measure of the total semiconductor device requirement, thus an important cost indicator of an inverter system:

\[
\text{Total average SDP} = (SDP)_{av} = \frac{\sum_{M=1}^{N} V_m I_m}{M_{av}}
\]

\[
\text{Total peak SDP} = (SDP)_{pk} = \frac{\sum_{M=1}^{N} V_m I_m}{M_{peak}}
\]

where, \( I_m_{av}, I_m_{peak} \) = The average and peak currents through the device respectively

\( V_m \) = The peak voltage induced on the device.

The average and peak SDPs of proposed inverter can be calculated for the given typical values {\( P_o = 150 \) W, \( M = 1, \cos \varnothing = 1 \)} as:

\[
(SDP)_{av} = \frac{2P_o (2 - \sqrt{3}M)}{\sqrt{3}M - 1} + \frac{4\sqrt{3}P_o}{\cos \varnothing \pi} \]

\[
(SDP)_{pk} = \max \left( \frac{4P_o}{\sqrt{3}M - 1} \right) + \frac{4P_o}{\cos \varnothing M}, \left( \frac{8P_o}{\cos \varnothing M} \right)
\]

Reliability evaluation: Reliability analysis of the proposed inverter can be found out in terms of mean time to failure.

IGBT Reliability (\( \lambda_p \)) is expressed (Xue et al., 2012) as:

\[
\lambda_p_{\text{IGBT}} = \lambda_b \pi_T \pi_A \pi_R \pi_S \pi_Q \pi_E \text{ failure/10}^6 \text{ h}
\]

The typical values for the proposed inverter are listed as: base failure rate, \( \lambda_b = 0.00074 \); junction temperature factor, \( \pi_T = 5.9 \); application factor, \( \pi_A = 0.7 \); power rating factor, \( \pi_R = \text{P}^{0.37} \); voltage stress factor, \( \pi_S = 1 \), quality factor, \( \pi_Q = 2.4 \), environment factor, \( \pi_E = 6.0 \):

\[
\lambda_p_{\text{IGBT}} = 0.00074 \times 5.9 \times 0.7 \times 35.08 \times 1 \times 0.7 \times 6.0 = 0.45028 \text{ failure/10}^6 \text{ h}
\]

Using 6 IGBT’s in the proposed inverter, the reliability can be calculated as:

\[
\lambda_p_{\text{inv}} = 6 \times 0.4502 \text{ failure/10}^6 \text{ h} = 2.70172 \text{ failure/10}^6 \text{ h}
\]

Mean Time to Failure (MTTF) for the system use in full life period is expressed as inverse of failure rate and, calculated as:

\[
\text{MTTF} = \frac{1}{\lambda} = 1/2.7017 \text{ failure/10}^6 \text{ h} = 10^6/2.7017 \text{ h} = 37, 01, 373 \text{ h} = 60.36 \text{ years}
\]

Thus the reliability (estimated life) of the proposed inverter is theoretically calculated to be 60.36 years.

**SIMULATION RESULTS**

To verify the operation of proposed inverter, simulations are performed in MATLAB/SIMULINK environment, where the solver is chosen as variable step discrete with step of 1.0 µs with following PV system input voltages of values: \( V_1, V_2, V_3 = 12 \) V and \( V_4 = 24 \) V, collectively, \( V_{dc} = 60 \) V; \( L_1 \) to \( L_8 = 2 \) mH \( C_1, C_4 = 10 \) µF and switching frequency, \( f_s = 20 \) kHz employing 120° switching scheme with a modulation index of value one. The output ac voltage waveforms (peak value) obtained through simulation for the proposed inverter are around 100 V in all the phases A, B and C, respectively which are observed with LC filter as shown in Fig. 6 and 7 shows the switching sequence of the switches \( S_1 \) to \( S_6 \). Table 1 provides a list of simulation parameters for the proposed inverter.

![Simulated output voltage waveforms of proposed inverter observed with LC filter (Scale: Y axis: 50 V/div)](image-url)
Fig. 7: Switching sequence of the proposed inverter (S₁ to S₆).

Fig. 8: Simulated capacitor waveforms (C₁ to C₄) (capacitor voltage values are given in the text).

Table 1: Simulation parameters of the proposed modified embedded switched inductor ZSI

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input DC voltage</td>
<td>60 V</td>
</tr>
<tr>
<td>Z-source network</td>
<td>L₁, L₂: 2 mH</td>
</tr>
<tr>
<td></td>
<td>C₁, C₂: 10 µF</td>
</tr>
<tr>
<td>Switching frequency, fₛ</td>
<td>20 kHz</td>
</tr>
<tr>
<td>Three phase output filter</td>
<td>L₃: 10 mH</td>
</tr>
<tr>
<td></td>
<td>C₃: 2000 µF</td>
</tr>
<tr>
<td>Three phase resistive load, R₆</td>
<td>10 Ω/phase</td>
</tr>
</tbody>
</table>

Figure 8 shows the capacitor voltage waveforms connected to the inverter having the values as 32.66 V in the capacitors Vₐ₁ and Vₐ₂, where Vₐ₃ and Vₐ₄ have 21.93 V and 18.43 V respectively. The obtained value shows that the internal capacitors C₃ and C₄ are under reduced stress condition, which is the notable feature of this proposed topology. Figure 9 shows the inductor current waveforms of values Iₜ₁ = 3.245 A, Iₜ₃ = 3.252 A.
Experimental results: Simulation results are verified through the experimental setup as shown in Fig. 10. In this model, four PV panels each rated for 37 W are connected at four different locations to produce a voltage of 60V. The dc sources are embedded within the switched inductor network, connected to the main inverter circuit to feed the load. The switching pulses of
the main inverter circuit are given from PWM pulse generating circuit employing 120° PWM control strategy. Shoot through pulses to turn ON the switches of the same phase leg are obtained through a separate circuit which is connected to the main PWM pulse generator circuit.

Figure 11 shows the various operating units like PWM pulse generator, shoot through pulse generator, isolation opto-coupler and impedance network are assembled to form the hardware of the proposed inverter. Various IC’s and passive elements are used to build the proposed inverter. It has IC MCT2E for isolation purposes. LM358P, HEF40106BP, CD4071BCN, HEF40718P are used to produce the pulses for the shoot through operations. Control signals for inverter switching operation with 120° phase shift are obtained through IC’s TL084CN, LM358N and HCF408LBE to produce reference, triangle carrier and PWM pulses, respectively. Output phase voltage reaches 88 and 70 V, respectively, when observed without and with filter through the digital signal oscilloscope as shown in Fig. 12 and 13. It is also observed that the voltage stress across the capaciters is reduced as shown in Fig. 14. Switching pulses given to the inverter terminals are shown in Fig. 15. Waveforms
of reference, carrier and PWM signals captured for a single switch are shown in Fig. 16 and the shoot through pulse for a single switch is shown in Fig. 17.

CONCLUSION

A novel modified embedded switched inductor ZSI is proposed for solar photo voltaic applications. Simulations are carried out by employing 120° pulse width modulation scheme. Hardware, for the proposed inverter is implemented. The simulation and hardware results agree to a great extent. The proposed inverter exhibits better performance and is most suitable for solar PV applications.

REFERENCES


