Analysis and Evaluation of Using a Tuning Inductance on the Performance of Gilbert Cell-Based CMOS Sub-Harmonic Mixer

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Abstract: The effect of using a tuning inductance on the performance of a Gilbert cell-based two level transistor CMOS sub-harmonic mixer is investigated. The tuning inductor used between the RF and LO switching stages causes conversion gain enhancement and noise figure improvement. Additionally, it compensates LO distortion due to the phase mismatch of LO signals in the sub-harmonic mixer. The design procedure is done in 0.18 μm CMOS process at 1.8 V supply voltage and 2.4 GHz frequency and reveals that the mixer has exhibited high performance after a FOM-based comparison, without increase the power consumption of 5 mW. The inductive connection between the RF and LO stages causes 7 dB enhancement of conversion gain and 7.3 and 6 dB improvement of noise figure and LO distortion, respectively while the mixer has achieved up to 8 dB conversion gain, 0.5 dBm IIP3, and 13.8 dB noise figure.

Key words: Conversion gain, noise figure, sub-harmonic mixer, tuning inductance

INTRODUCTION

Recently, several low power receiver architectures based on single chip CMOS have been presented that among of them Direct-Conversion Receivers (DCRs) are suitable candidates for low cost and low power single chip integration. However, DCRs have disadvantages such as Local Oscillator (LO) self mixing and leakage, large dc offset, and 1/f noise that can seriously degrade the performance of the receiver. Several techniques have been proposed in order to combat these problems such as using a frequency doubler at the output of the LO (Karanicolas, 1996) and using a sub-harmonic mixer. In a sub-harmonic mixer, the LO frequency is internally multiplied and the mixer uses higher order harmonics of the LO signal for up or down conversion. Lower LO frequency significantly simplifies transceiver design and hence, it can be used to build integrated RF front-ends for high frequencies. Numerous sub-harmonic mixers were developed based on the diode nonlinearity (Shimozawa et al., 1998; Matinpour and Laskar, 1999). However, these mixers suffer from low conversion gain and require high LO power, isolator blocks, and filters that make them difficult to integrate. Sub-harmonic mixers based on the modified Gilbert cell were presented in (Wu et al., 2007; Syu and Meng, 2009; Hsu and Lee, 2006; Kodkani and Larson, 2007; Svtiek and Raman, 2004; Sheng et al., 2000) in which an additional level of LO switching stage and quadrature LO signals were used to generate the double frequency component and mix with the RF signal. Since, this technique needs three levels of transistors consisting one RF and two LO stages, it is not suitable for low voltage applications and suffers from high power consumption and poor linearity.

On the other hand, the requirement of linearity performance for a mixer becomes more critical criteria in RF receivers and affects the linearity of the overall system. This requirement is approximately proportional to the dc power consumption and decreases heavily with the supply voltage reduction. Therefore, it is a great challenge to achieve high linearity at low power and low voltage.

With regards to the above consideration, this study intends to provide an analysis and investigation of using a tuning inductance on the performance of a CMOS sub-harmonic mixer.

MIXER STRUCTURE AND DESIGN CRITERIA

The transistor level schematic of the proposed CMOS sub-harmonic mixer is shown in Fig. 1 in which the positions of LO and RF stages have been exchanged. The mixer is similar to its BiCMOS approach presented in (Nimmagadda and Rebeiz, 2001) except the inductor used between the RF transconductance and LO switching stages. It consists of the LO switching stage (M1-M4), RF transconductance stage (M5-M8), tuning inductors \( L_e \) between LO and RF stages, and output load stage. The LO stage is actually a frequency doubler and the currents through it which are equal to the currents through the inductors \( L_e \) are switched at twice the LO frequency. So, for using at the 2.4 GHz band, the gates of LO stage transistors are driven by 1.2 GHz quadrature signals with
relative phase shifts of 0°, 90°, 180°, and 270° to effectively provide switching at twice the rate of the traditional cells. Moreover, to achieve the best noise and conversion gain performance and to make the LO stage transistors as ideal switches, these transistors are biased in the saturation region close to the triode one in order to minimize their switching time.

RF transconductance stage is in anti-parallel configuration with respect to the output or IF port while the LO switching stage is isolated from the IF port by RF differential pairs. This configuration avoids the direct coupling from the LO to RF stage, which is the origin of self-mixing, and also provides good RF-to-IF and LO-to-IF port isolation. Large parasitic capacitances loading the common source of RF stage cause critical drawbacks and must be tuned out. These capacitances are nonlinear and can be charged and discharged by the offset voltage generated by mismatch and degrade the mixer linearity. In addition, they lead to reduction of the transconductance gain and cause the flicker noise such that the conversion gain and noise figure of the mixer are degraded. A simple and very effective method has been used in the proposed mixer in order to tune out these capacitances by utilizing the inductor $L_e$ between the LO and RF stages. The equivalent circuit which consists of parasitic capacitances $C_{p,\text{total}}$ and the tuning inductor $L_e$ is shown in Fig. 2. $L_e$ in parallel with $C_{p,\text{total}}$ resonates at the desired LO frequency, which is twice the applied LO frequency, and hence the charging and discharging of the noise voltage is suppressed leading to a significant reduction of noise figure. In addition, due to the fact that the tuning inductor provides large impedance at the desired LO frequency, the LO voltage swing at the common source of the RF transistors, $V_{\text{c}}$, is larger than the common drain of the LO transistors, $V_{\text{dc}}$, that causes higher conversion gain at lower LO power than would be required without the tuning inductor.

![Fig. 1: Schematic of the proposed mixer](image-url)

**LO DISTORTION IMPROVEMENT**

Another benefit of using the tuning inductor is that with presence of $L_e$, LO distortion due to the phase mismatch of LO signals is improved. We assume that the LO signals driving the gates of LO stage transistors are as below:

$$
\begin{align*}
V_{\text{LO}0} &= \frac{a}{2} \cos(\omega_{\text{LO}}t) \\
V_{\text{LO}90} &= \frac{a}{2} \cos(\omega_{\text{LO}}t + \frac{\pi}{2} + \theta_1) \\
V_{\text{LO}180} &= \frac{a}{2} \cos(\omega_{\text{LO}}t + \pi + \theta_1) \\
V_{\text{LO}270} &= \frac{a}{2} \cos(\omega_{\text{LO}}t + \frac{3\pi}{2} + \theta_2 + \theta_1)
\end{align*}
$$

where, $\theta_1$ and $\theta_2$ are phase mismatch of LO signals. According to the MOS square-law current relation, the currents of transistors M1-M4 can be written as:

$$
\begin{align*}
I_1 &= \frac{\beta_n}{2} \left[ \frac{a^2}{8} \cos(2\omega_{\text{LO}}t) + \Delta V_a \cos(\omega_{\text{LO}}t) + \frac{a^2}{8} + \Delta V^2 \right] \\
I_2 &= \frac{\beta_n}{2} \left[ \frac{a^2}{8} \cos(2\omega_{\text{LO}}t + 2\theta_1) - \Delta V_a \cos(\omega_{\text{LO}}t + \theta_1) + \frac{a^2}{8} + \Delta V^2 \right] \\
I_3 &= \frac{\beta_n}{2} \left[ \frac{a^2}{8} \cos(2\omega_{\text{LO}}t + 2\theta_2) - \Delta V_a \sin(\omega_{\text{LO}}t + \theta_2) + \frac{a^2}{8} + \Delta V^2 \right] \\
I_4 &= \frac{\beta_n}{2} \left[ \frac{a^2}{8} \cos(2\omega_{\text{LO}}t + 2\theta_1 + 2\theta_2) + \Delta V_a \sin(\omega_{\text{LO}}t + \theta_1 + \theta_2) + \frac{a^2}{8} + \Delta V^2 \right]
\end{align*}
$$

where, $\beta_n = \mu_n C_{\text{ox}} W/L$, $\Delta V = V_{\text{GS}} - V_{Tn}$, and $V_{Tn}$ is the transistor threshold voltage. Therefore, the differential current driving the transconductance stage of the mixer is equal to:

$$
\begin{align*}
I_{i1} - I_{i2} &= (I_1 + I_2) - (I_3 + I_4) = \frac{\beta_n a^2}{2} \left[ (1 + \cos(2\theta_1)) (\cos(2\omega_{\text{LO}}t) + \cos(2\omega_{\text{LO}}t + 2\theta_1)) \right. \\
&- \frac{a^2}{8} \sin(2\theta_1) (\sin(2\omega_{\text{LO}}t) + \sin(2\omega_{\text{LO}}t + 2\theta_1)) \\
&+ \Delta V_a (1 - \cos(\theta_1)) (\cos(\omega_{\text{LO}}t) + \sin(\omega_{\text{LO}}t + \theta_1)) \\
&\left. + \Delta V_a \sin(\theta_1) (\sin(\omega_{\text{LO}}t) - \cos(\omega_{\text{LO}}t + \theta_1)) \right]
\end{align*}
$$
As it can be seen, in addition to the desired LO frequency, $2\omega_{LO}$, the differential current consists of the applied LO frequency, $\omega_{LO}$, which is due to the phase mismatch of LO signals. This unwanted harmonic affects the phase noise of the LO and degrades the noise figure of the overall circuit.

In order to consider the effect of tuning inductor, LO distortion level parameter is defined as unwanted to wanted harmonics of the differential current. Hence without the tuning inductor, LO distortion can be derived as follow:

$$\text{LO distortion} = \frac{\text{Unwanted Harmonic Power at } \omega_{LO}}{\text{Wanted Harmonic Power at } 2\omega_{LO}}$$

$$= \frac{64\Delta V^2 (1-\cos(\theta_1))(1+\sin(\theta_2))}{a^2 (1+\cos(2\theta_1))(1+\cos(2\theta_2))}$$

Since the tuning inductor makes different impedances versus frequency, the level of unwanted harmonic will be attenuated at the common source node of the transconductance stage. So, the level of LO distortion in case of utilizing $L_e$ is given by:

$$\text{LO distortion}_{L_e} = \frac{16\Delta V^2 (1-\cos(\theta_1))(1+\sin(\theta_2))}{a^2 (1+\cos(2\theta_1))(1+\cos(2\theta_2))}$$

According to Eqs. (4) and (5), the tuning inductor causes a reduction in the LO distortion by a factor of 4 and hence improves LO distortion of the sub-harmonic mixer.

**SIMULATION RESULTS**

The proposed mixer is designed and simulated by Advanced Design System in 0.18 μm CMOS process at 1.8 V supply voltage. The RF signal at 2.41 GHz is down converted to 10 MHz through a 1.2 GHz LO signal.
The simulated conversion gain as a function of LO power without and with the tuning inductor $L_e$ is shown in Fig. 3a and b. As can be seen, by using the tuning inductor the conversion gain has been increased by 7 dB and has reached to its maximum value of 8 dB at 0 dBm LO power.

The comparison of DSB noise figure without and with $L_e$ is shown in Fig. 4a and b. The noise figure is 21.1 and 13.8 dB without and with $L_e$, respectively at 20 MHz IF frequency which indicates 7.3 dB improvement.

Third-order Input Intercept Point (IIP3) is simulated at the input RF frequency of 2.4095 and 2.4105 GHz.

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<tr>
<td>Technology (µm)</td>
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<td>0.35</td>
<td>0.18</td>
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<td>0.18</td>
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<td>2.2</td>
<td>5.25</td>
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<td>12.7</td>
<td>6.57</td>
<td>1.35</td>
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<td>Conversion gain (dB)</td>
<td>14.5</td>
<td>9</td>
<td>14.5</td>
<td>4.5</td>
<td>8.9</td>
<td>9.17</td>
<td>8</td>
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<tr>
<td>IIP3 (dBm)</td>
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<td>-4</td>
<td>-17.92</td>
<td>0</td>
<td>-11.66</td>
<td>-5.01</td>
<td>0.5</td>
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<tr>
<td>Noise figure (dB)</td>
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<td>14</td>
<td>20.34</td>
<td>11</td>
<td>24</td>
<td>30.5</td>
<td>13.8</td>
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<tr>
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<td>4.72</td>
<td>5.22</td>
<td>-8.56</td>
<td>-4.71</td>
<td>8.46</td>
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with 1 MHz separation and as it is shown in Fig. 5, the IIP3 has achieved up to 0.5 dBm.

A plot of LO distortion versus phase mismatches $\theta_1$ and $\theta_2$ with and without $L_e$ is shown in Fig. 6. As it can be seen, LO distortion does not change significantly as $\theta_1$ increases and $\theta_2$ is the main source of poor LO rejection. Using the tuning inductor causes an improvement of 6 dB for LO distortion.

Table 1 provides comparison between performance of the proposed mixer and the most recently published works (Wu et al., 2007; Syu and Meng, 2009; Huang et al., 2005; Jen et al., 2006; Huang et al., 2006; Lee et al., 2005). A Figure of Merit (FOM) which is defined in Eq. (6) is adopted here to compare the performance of different mixers by evaluating the effects of the conversion gain, noise figure, linearity and power dissipation.

$$FOM = 10 \log \left( \frac{10^{(CG/20)} \cdot 10^{(IIP3-10)/20}}{10^{NF/10} \cdot P_{diss}} \right)$$

where Conversion Gain (CG) and Noise Figure (NF) are expressed in dB, IIP3 in dBm, and power dissipation in wattage. A higher FOM indicates a better performance for a mixer. The measured FOM of the proposed mixer without and with the tuning inductor $L_e$ is -1.08 and 8.46 and shows that by utilizing the tuning inductor between the LO and RF stages of the mixer, the linearity, conversion gain, and noise figure have been improved without increase the power dissipation of 5 mW.

**CONCLUSION**

In this study, the effect of using a tuning inductance on the performance of a Gilbert cell-based two level transistor CMOS sub-harmonic mixer is investigated. The tuning inductor used between the RF and LO switching stages has improved the noise figure and enhanced the conversion gain of the mixer. Additionally, it has compensated LO distortion due to the phase mismatch of LO signals in the sub-harmonic mixer. Full transistor level simulation done in 0.18 $\mu$m CMOS process at 1.8 V supply voltage has shown that the proposed mixer has exhibited high performance after a FOM-based comparison, without increase the power consumption.

**REFERENCES**


