Research Article Comparison between 7-Level Cascaded and 7-Level Diode-Clamped Multilevel Inverters for Feeding Induction Motor

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Abstract: In this study, two types of multilevel convertors, cascaded multilevel inverter with separate DC sources and diode clamped multilevel inverter with common DC source are modeled and compared in the case of feeding of an induction motor. Here, SHEPWM technique is used as the switching strategy. Also a new variable torque feedback control on modulation index is presented, to preserve the induction motor in stable condition. Furthermore, the merits and demerits of each convertor from power quality point of view are compared. Outputs of simulations shows that despite of that feeding of loads using diode clamped multilevel convertors with common dc source is easier than cascaded converters from feeding inverters with DC sources point of view, even thought cascaded multilevel inverters has more robust performance in case of feeding variable torque induction motor loads. And our feedback controller works to improve outputs of multilevel inverter and parameters of induction motor in both cases.

Keywords: Cascaded 7-level inverter, diode clamped 7-level inverter, induction motor

INTRODUCTION

Nowadays, there are many applications for multilevel inverters, such as Flexible AC Transmission Systems (FACTS), High Voltage Direct Current (HVDC) transmission, electrical drives and Dispersed Generation (DG) systems. In some applications the convertor connects one DC source to the network and some other applications; they can connect separate DC sources to the network.

There are different types of multilevel inverters, but three of them are important and used in industrial applications; capacitor clamped multilevel inverter, diode clamped multilevel inverter and cascaded multilevel inverter with separate DC sources. Each multilevel inverter consists of an array of power semiconductors and capacitors and generates AC voltages. Proper switching of switches permits the addition of capacitor voltages in the output port an results in high voltage generation without stressing the semiconductors (José *et al.*, 2002) (Fig. 1).

In some cases, it is impossible to have several separate DC buses; or in some industrial applications, due to the economic considerations the power system must be designed just by one DC bus. Furthermore when the system has several DC sources, because of some reasons like shadow affect in PVs the system, DC-source fault can destroy the output voltage of cascaded multilevel, but in diode clamped using a voltage control on common Babur this effect decreases. So the modeling of different types of multilevel especially for those that are usually used in industrial applications and comparison between these schemes should be studied and discussed.

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In Nabae *et al.* (1981) has introduced diode clamped multilevel inverter in 1981. It has improved over the time. In Adam *et al.* (2011), Adam has proposed an improved version of the conventional flying capacitor multilevel inverter that replaced flying capacitors with half or full bridge cells. A novel H-bridge multilevel pulse width modulation for cascaded multilevel based on series connection of high voltage diode clamped inverter and low-voltage conventional inverter has been proposed in Alireza *et al.* (2011).

In this study, topologies, switching strategies and advantages of diode clamped and cascaded multilevel inverters are discussed. Furthermore, modeling of 7level diode clamped and 7-level cascaded multilevel inverter and their control strategies for supplying an induction motors are presented. Finally the electrical feeding of a variable torque induction motor load by these inverter schemes, using a feedback control on modulation index are simulated and then outputs are analyzed.

MULTILEVEL TOPOLOGIES

Diode-clamped multilevel inverter: One phase of a seven level diode clamped inverter is shown in Fig. 2. As it is shown in the circuit, in this type of multilevel

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Fig. 1: Addition of the capacitor voltages in multilevel inverters (José *et al.*, 2002)



Fig. 2: One phase of diode-clamped 7-level inverter

Tabla	1.	Switching	nattern	of 7 level	diada	clamped	inverte

	C1	62	62	<u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u></u>	0.5	64	67	C 0	50	610	611	612
	51	52	33	54	33	30	3/	30	39	510	511	512
Vdc/2	1	1	1	1	1	1	0	0	0	0	0	0
Vdc/3	0	1	1	1	1	1	1	0	0	0	0	0
Vdc/6	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	0
-Vdc/6	0	0	0	0	1	1	1	1	1	1	0	0
-Vdc/3	0	0	0	0	0	1	1	1	1	1	1	0
-Vdc/2	0	0	0	0	0	0	1	1	1	1	1	1

we have only one DC-source and the DC-bus is split into N level by N-1 capacitors. Here N = 7 and we have six capacitors. The output phase voltage has seven levels: Vdc/2, Vdc/3, Vdc/6, 0, -Vdc/6, -Vdc/3, -Vdc/2.

There are ten diodes (Dc1-Dc10). These diodes clamp the switching voltage to half level of the dc-bus voltage. The neutral point N is considered as the reference point (Qiang and Wenhua, 2009). To produce a seven-level voltage, seven switch combinations must be used. Table 1 shows the switching pattern of each



Fig. 3: Output phase voltage of cascaded 7-level inverter (José et al., 2002)

level. Although each active switching device is only required to block a voltage level of Vdc/ (m-1), the clamping diodes must have different voltage rating for reverse voltage blocking (José *et al.*, 2002).

In some cases this voltage reach to 2/3Vdc. So if diodes with same voltage rating as the active devices are used, the number of required diodes for each phase will be (m-1) (m-2). This number represents a quadratic increasing and when m is sufficiently high, the number of diodes required will make the system impractical to implement and if the inverter runs under PWM, the diodes reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications (José *et al.*, 2002).

CASCADED MULTILEVEL INVERTER

Cascaded multilevel inverter (Fig. 3) has advantages that have been presented in Alireza *et al.* (2011). Least components, absence of extra clamping diodes or voltage balancing capacitors and easy adjustment of the number of output voltage level are some of them. Furthermore switching devices turn on and off only once per cycle to overcome the switching loss problem (Kavousi *et al.*, 2012).

The cascaded multilevel inverter consists of a series of H-bridge (single-phase full-bridge) inverter units. Each full-bridge can generate three different voltage outputs, $+V_{dc}$, 0 and $-V_{dc}$. However, all type of multilevel inverters can produce staircase waveform (Nami *et al.*, 2011). The number of output phase voltage levels in a cascaded multilevel inverter is 2S+1, where S is the number of dc sources. For example, phase voltage waveform for a 7-level cascaded multilevel inverter with three isolated DC sources (S=3) is shown in Fig. 4.

SELECTIVE HARMONIC ELIMINATION PWM (SHEPWM)

In this study, SHEPWM technique is used as control for the switches of multilevel inverter. A 7level inverter waveform shown in Fig. 4 has three



Fig. 4: One phase of cascaded 7-level inverter



Fig. 5: Control block of multilevel inverters

variables, θ_1 , θ_2 and θ_3 , where, V_{dc1} , V_{dc2} and V_{dc3} are assumed to be equal. Considering equal amplitude of all dc sources, the Fourier series expansion of the output

$$V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n \,\omega t)$$
(1)

where, V_n is the amplitude of n^{th} harmonic. Switching angles are limited between zero and $\pi/2$ ($0 \le \theta_i < \pi/2$). Because of odd quarter-wave symmetric characteristic, harmonics with even order become zero. Consequently, V_n becomes:

$$V_n = \begin{cases} \frac{4V_{dc}}{n\pi} \sum_{i=1}^{S} \cos(n\theta_i) & \text{for odd ns} \\ 0 & \text{for evenns} \end{cases}$$
(2)

The control block for these two models, the cascaded and diode clamped multilevel inverter, is shown in Fig. 5. It has to input from outside, m and a clock time to produce w. this block produces 36 pulses at each scheme; 12 pulses per phase. There is a code in each of three boxes at the middle of Fig. 5 that produce final switching pulses.

ASYNCHRONOUS MACHINE (INDUCTION MOTOR LOAD)

Asynchronous machines are widely used in industries. Induction motors have their characteristic during starting and fault conditions (Hagiwara *et al.*, 2010; Hatti *et al.*, 2009). At this study a kind of squirrel cage asynchronous machine from the library of MATLAB/Sims Power is used as a load for our multilevel inverters. Then two signals, Rotor Current and Rotor Speed torque are used for analyzing the conditions of induction motor in each case. Figure 6 to 8 show outputs at the case of using ideal ac source. Here the electromagnetic torque is also presented.

SIMULATION RESULTS

Figure 6 to 8 showed the outputs of an ideal case with ideal AC source. Here the output voltage and harmonic spectrum of each inverter that is used for feeding this load are showed. In Fig. 6 to 8 the results with the torque of 12N.m. are showed. At this study the torque is change up to 20N.m. Figure 9 to 10 show the output voltages of Cascaded and Diode-Clamped multilevel inverter.

As Fig. 11 shows, using SHPEWM technique the 5^{th} and 7^{th} harmonic are eliminated here. THD parameter of the first type is 22.99% and for the second one is 23.2%. These magnitudes are almost equal. This equality is because of using same control box and a little setting in the control strategy that allow us to



Fig. 6: Rotor current of induction motor using an ideal ac source



Fig. 7: Rotor speed of induction motor using of ideal ac source



Fig. 8: Electromagnetic torque of induction motor using of ideal ac source

compare the results of this two case as sources for feeding an induction motor. In this research the induction motor is fed with a three phase 220volt AC voltage source. In the case of cascaded multilevel it must be fed with three separate 73.3 volt voltage bus bars and in the case of DCML inverter it uses a single 440 volt voltage bus bar to produce proper voltage. A 7-level DCML has six internal capacitors that divide the DC voltage to six parts and in this case each capacitor earns 73.3 volt too.



Fig. 9: Output voltage of cascaded 7-level inverter



Fig. 10: Output voltage of Diode-Clamped 7-level inverter



Fig. 11: Harmonic spectrum of cascaded 7-level inverter

Figure 12a shows the rotor current of induction motor in the case of feeding load with cascaded 7-level inverter at the torque of 12 Nm, Fig. 12b shows this parameter at the torque of 20 Nm without using any control; and Fig. 12c shows this parameter at the torque of 20 Nm with a kind of simple feedback control on modulation index.

Fig. 13a shows the rotor speed of induction motor in the case of feeding load with cascaded 7-level inverter at the torque of 12 Nm, Fig. 13b shows this parameter at the torque of 20 Nm without using any control and Fig. 13c shows this parameter at the torque of 20 Nm with a feedback control on modulation index.



Fig. 12: (a) Rotor current with 12Nm in case of feeding cascaded 7-level inverter, (b) Rotor current with 20Nm without control and (c) Rotor current with 20Nm by feedback control



Fig. 13: (a) Rotor speed with 12Nm in case of feeding with cascaded 7-level inverter, (b) Rotor speed with 20nm without control and (c) Rotor speed with 20Nm by feedback control

After increasing the torque without control a little change (about +1%) in THD is seen and using feedback control it will be improved.

Figure 14a shows the rotor current of induction motor in the case of feeding load with diode clamped 7-level inverter at the torque of 12 Nm, Fig. 14b shows



Fig. 14: (a) Rotor current with 12Nm in case of feeding with diode-clamped 7-level inverter, (b) Rotor current with 20Nm without control and (c) Rotor current with 20Nm by feedback control



Fig. 15: (a) Rotor speed with 12N.m in case of feeding with Diode-clamped 7-level inverter, (b) Rotor speed with 20Nm. without control and (c) Rotor speed with 20N.m by feedback control

this parameter at the torque of 20 Nm without using any control; and Fig. 14c shows this parameter at the torque of 20 Nm with a kind of simple feedback control on modulation index.

And Fig. 15a, b and c show the rotor speed of induction motor with the torque of 12 Nm, rotor speed with 20 Nm torque without control and this parameter using a feedback control on modulation index, respectively. And in this case, increase in torque change THD about +2% and using this feedback control improves THD like previous case.

CONCLUSION

As Fig. 9 to11 show using SHPMW technique, an acceptable AC voltage and tolerable THD percentage (about 23%) was earned. In this model 5th and 7th harmonics are eliminated.

Moreover as it was mentioned in the case of uncontrolled multilevel, with increased torque from 12Nm to 20Nm the THD of DCML is a little higher than the THD of cascaded multilevel.

Figure 12a shows that the time of end of transient state of rotor current is around 0.4 sec in ideal feeding; then in Fig. 12b this time for uncontrolled cascaded inverter is 1.2sec and in Fig 12c it is 0.44 sec. so here the control of modulation index is practical and adjusts the output. Figure 14a and b show that this time for the case of DCML, is 0.44 and after increasing of torque it changes to 1.4sec and with a controller for variable torque it adjusts to 0.75sec. But it can be observed in these figures that cascaded multilevel inverters are more robust than diode clamped schemes against changing in torque.

Figure 15b shows that in case of DCML changing in torque can causes a downfall in rotor speed and it is not as robust as the case of cascaded multilevel. In this case with this magnitude of torque induction load lost.

Furthermore a simple feedback control on modulation index has been used for better feeding of an induction motor in case of changing torque. This PI controller eventuates significant improvement in parameters.

At overall view, using only one DC input bus bar is the most benefit of DCML in particular for DG uses that can decrease the problems of DC-source faults and it can decrease the required reserve capacitance. But at all using cascaded multilevel inverter because of fewer power electronic components, more simple controlling and being more robust against variable torques is recommended according to the results of this study.

REFERENCES

Adam, P., A. Bader, K.H. Ahmed, S.J. Finney and B.W. Williams, 2011. New flying capacitor multilevel converter. Proceeding of IEEE International Symposium on Industrial Electronics (ISIE), pp: 535-539.

- Alireza, N., Z. Firuz, G. Arindam and B. Frede, 2011. A hybrid cascade converter topology with seriesconnected symmetrical and asymmetrical diodeclamped H-Bridge cells. IEEE T. Power Electr., 26(1): 51-65.
- Hagiwara, M., K. Nishimura and H. Akagi, 2010. A medium-voltage motor drive with a modular multilevel PWM inverter. IEEE T. Power Electr., 25(7): 1786-1799.
- Hatti, N., K. Hasegawa and H. Akagi, 2009. A 6.6-kv transformerless motor drive using a five-level diode-clamped PWM inverter for energy savings of pumps and blowers. IEEE T. Power Electr., 24(3): 796-803.
- José, R., L. Jih-Sheng and Z.P. Fang, 2002. Multilevel inverters: A survey of topologies, controls and applications. IEEE T. Power Electr., 49(4): 724-738.
- Kaviani, A., S.H. Fathi, N. Farokhnia and A. Ardakani, 2009. PSO an effective tool for harmonics elimination and optimization in multilevel inverter. Proceeding of 4th IEEE Conference on Industrial Electronics and Applications. Xi'an, pp: 2902-2907.
- Kavousi, A., B. Vahidi, R. Salehi, M.K. Bakhshizadeh, N. Farokhnia and S.H. Fathi, 2012. Application of the Bee algorithm for selective harmonic elimination strategy in multilevel inverters. IEEE T. Power Electr., 27(4): 1689-1696.
- Nabae, A., I. Takahashi and H. Akagi, 1981. A New neutral-point-clamped PWM inverter. IEEE T. Ind. Appl., IA-17(5): 518-523.
- Nami, A., F. Zare, A. Ghosh and F. Blaabjerg, 2011. A hybrid cascade converter topology with seriesconnected symmetrical and asymmetrical diodeclamped H-Bridge cells. IEEE T. Power Electr., 26(1): 51-65.
- Qiang, S. and L. Wenhua, 2009. Control of a cascade statcom with star configuration under unbalanced conditions. IEEE T. Power Electr., 24(1): 45-58.
- Wanmin, F., R. Xinbo and W. Bin, 2009. A generalized formulation of quarter-wave symmetry She-PWM problems for multilevel inverters. IEEE T. Power Electr., 24(7): 1758-1766.