

Research Article

High Step-Up DC-DC Converter for Distributed Generation System

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Abstract: This study proposes a method which consists of High step up DC-DC converter with a coupled inductor for distributed generation system. Theoretically the conventional boost converter provides high step up voltage gain but in practical it is limited by reverse recovery problem of diode, effective series impedance of inductors and capacitors and switching losses. High charged current and conduction losses occur in the switch when voltage lift and switched capacitor techniques are used. In the proposed strategy a coupled-inductor and two capacitors is utilized to achieve high step-up voltage gain. High power loss and voltage spike on the switch is avoided using passive clamp circuit that recycles the leakage inductor energy. The operating principle and steady-state analysis are discussed. The Proposed topology was simulated using PSPICE SOFTWARE and the following results were obtained. For an input voltage of 24V, an output of 333V was obtained.

Keywords: Coupled inductor, DG System, high gain, passive clamp circuit

INTRODUCTION

Distributed Energy Resources (DERs) are becoming integral components of electric power distribution systems nowadays. Distributed generation, also called on-site generation, dispersed generation, embedded generation, generates electricity from many small energy sources. The DG system is mainly based on renewable energy resources. But, usually, the voltage output of these renewable sources is low and hence cannot be directly connected to the grid. Thus stepping up of voltage is necessary. Thus, in most of the cases, an isolated dc-dc converter forms part of the interface required to connect the DER output to the distribution system. The conventional boost converter is not good candidates for extremely high step-up applications, because the voltage gain is only determined by the duty cycle. This results in extreme duty cycles, which means very narrow turnoff pulses in high step-up conversions. Hence the conventional boost converter cannot provide such a high dc voltage gain even for an extreme duty cycle and also may result in serious reverse-recovery problems and increase the rating of all devices. As a result, the conversion efficiency is degraded and the Electromagnetic Interference (EMI) problem is severe under this situation (Mohan *et al.*, 1995).

In order to get high voltage gain and to increase the conversion efficiency, many modified boost converter topologies have been investigated in recent years. Abutbul *et al.* (2003) proposed a step-up switching-mode converter with high voltage gain using a

switched-capacitor circuit. This converter can achieve any voltage ratio and can operate at relatively low duty cycle. Thus the reverse recovery problem of diode can be reduced. But, the diode will have high voltage stress and switch will suffer high charged current. The conduction loss is also high. Da Silva *et al.* (2001) proposed a boost soft-single-switch converter. The proposed topology has only one single active switch. The converter is operated with soft switching in a Pulse-Width-Modulation (PWM) manner, hence the voltage and current stresses is low. But in order to achieve the soft switching the voltage gain is limited below four.

Jovanovic and Jang (1999) and Duarte and Barbi (2002) proposed voltage clamped techniques. Although voltage-clamped techniques are manipulated in the converter design to overcome the severe reverse-recovery problem of the output diode in high-level voltage applications, there still exists overlarge switch voltage stresses and the voltage gain is limited by the turn-on time of the auxiliary switch. Papanikolaou and Tatakis (2004) proposed using active voltage clamp circuits in flyback converters operating in continuous conduction mode under wide load variation. This topology provides isolation and also limits over voltages. A transformer is used and by adjusting the turn's ratio of the transformer, high step up voltage gain can be achieved. But the transformer is utilized during one half cycles only. Since voltage on secondary will be reflected onto the primary, high rating is required for the main switch.

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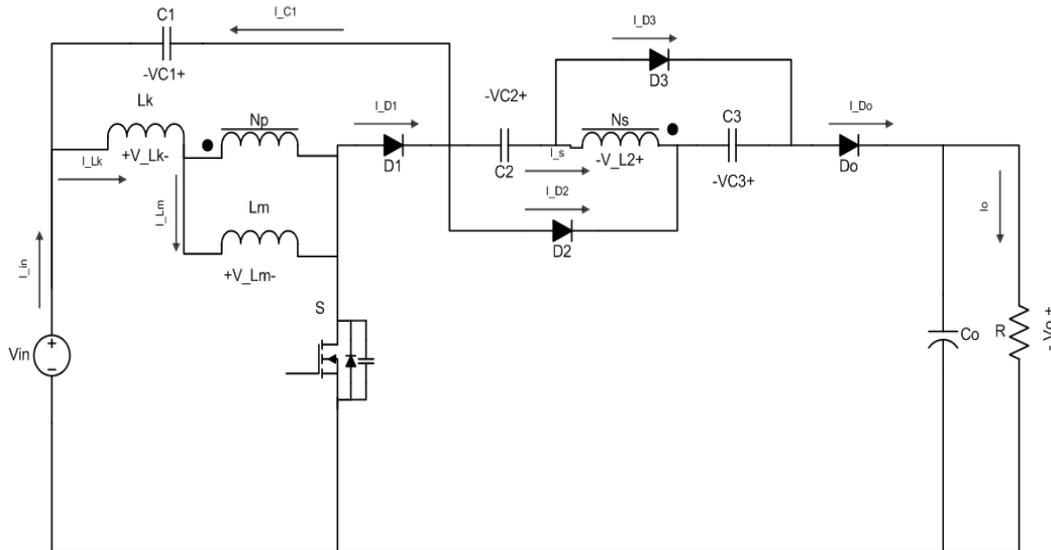


Fig. 1: Proposed topology

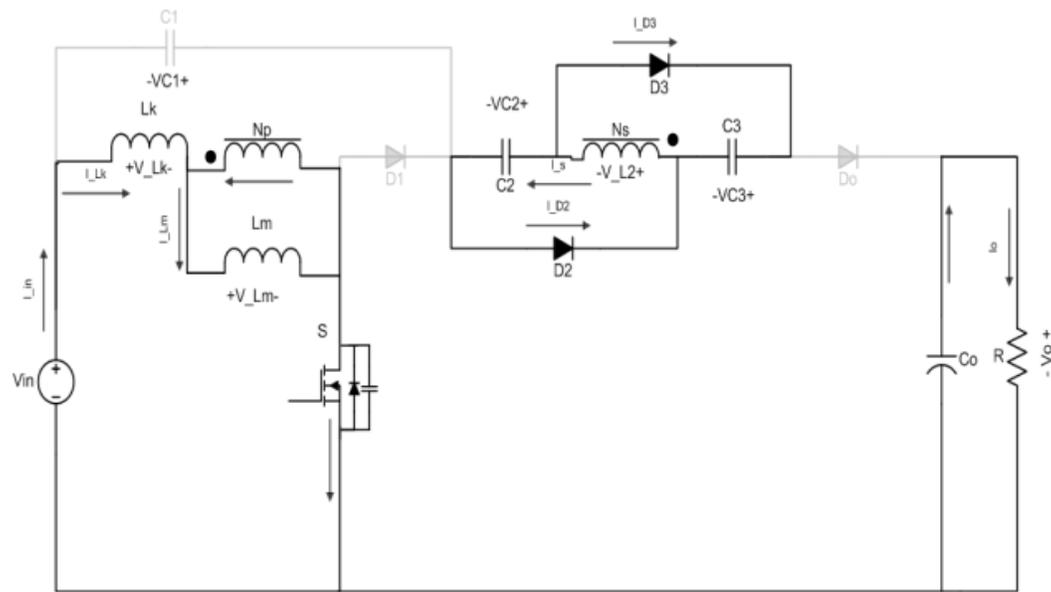


Fig. 2: Mode 1

In Hirachi *et al.* (2002) and Roh *et al.* (1999), coupled inductors were employed to provide a high step-up ratio and to reduce the switch voltage stress substantially and the reverse-recovery problem of the output diode was also alleviated efficiently. In this case, the leakage energy of the coupled inductor is another problem as the switch was turned off. It will result in the high-voltage ripple across the switch due to the resonant phenomenon induced by the leakage current. In order to protect the switch devices, either a high-voltage-rated device with higher or a snubber circuit is usually adopted to deplete the leakage energy. But the power conversion efficiency will be degraded.

Zhao and Lee (2003) proposed a high-efficiency, high step-up dc-dc converters by only adding one

additional diode and a small capacitor. It can recycle the leakage energy and alleviate the reverse-recovery problem. In this scheme, the magnetic core can be regarded as a flyback transformer and most of the energy was stored in the magnetic inductor. However, the leakage inductor of the coupled inductor and the parasitic capacitor of the output diode resonated after the switch was turned on, a proper snubber is necessary to reduce the output rectifier peak voltage.

In the proposed strategy a coupled-inductor and two capacitors is utilized to achieve high step-up voltage gain. High power loss and voltage spike on the switch is avoided using passive clamp circuit that recycles the leakage inductor energy. The operating principle and steady-state analysis are discussed.

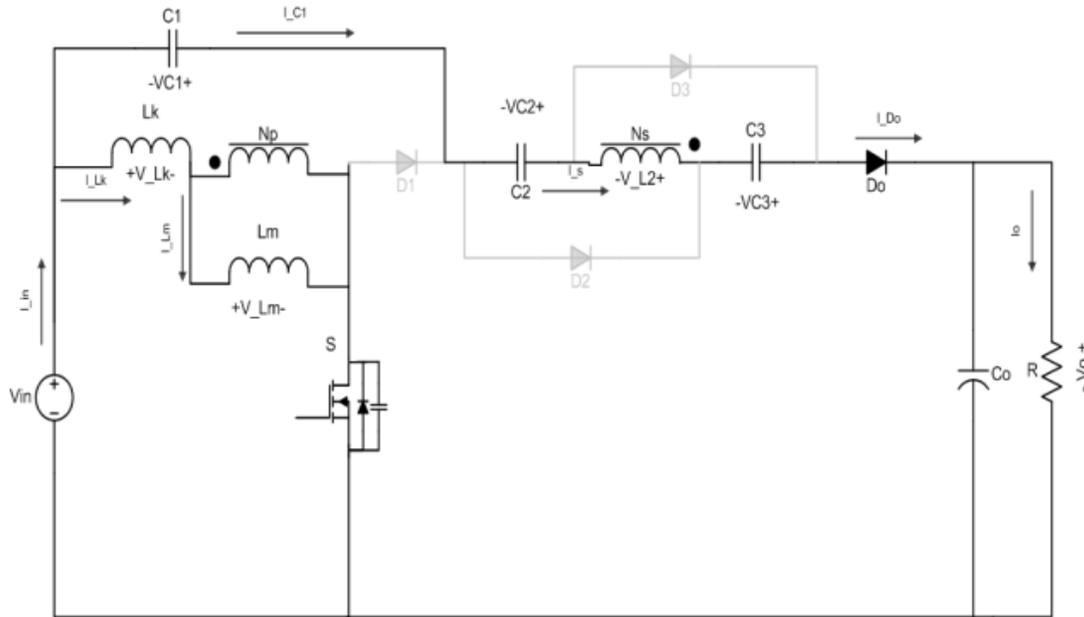


Fig. 3: Mode 2

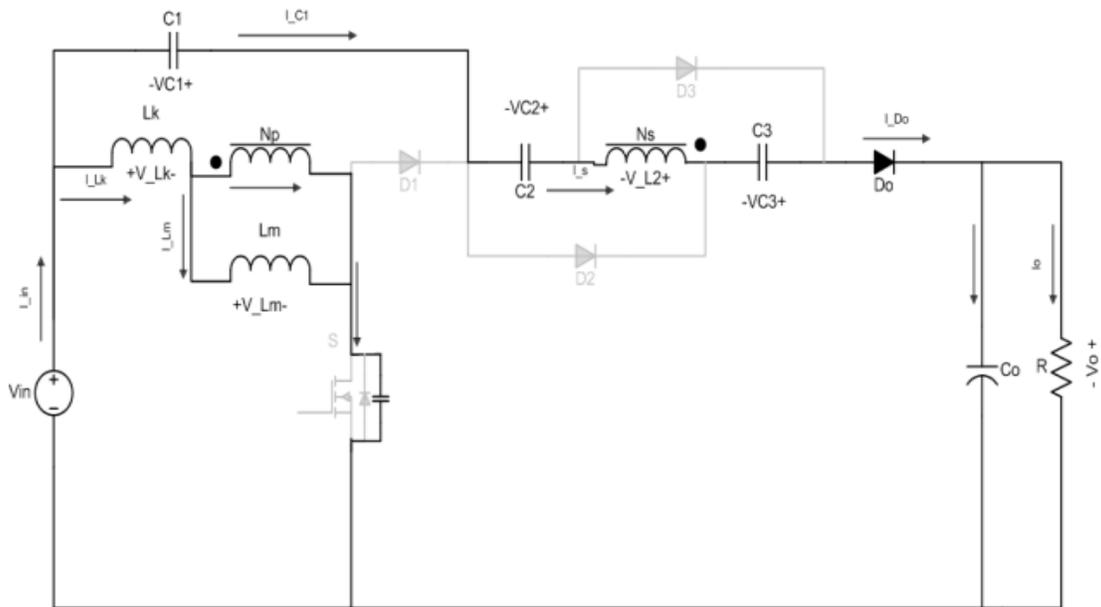


Fig. 4: Mode 3

OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Figure 1 shows the proposed circuit consists of DC input voltage V_{in} , main switch S, coupled inductor N_p and N_s , clamp diode D1 and clamp capacitor C1, two capacitors C2 and C3, diodes D2 and D3 and output diode D_o and output capacitor C_o as shown in Fig. 1. The capacitor C1 recycles the leakage inductor energy. This clamps the voltage across switch S thereby reducing the voltage stress on the switch. During switch turnoff and turn on the capacitors C2 and C3 are

charged in parallel and discharged in series by secondary side of coupled inductor. Magnetic inductor L_m is charged by the supply voltage V_{in} and the coupled inductor induces voltage on its secondary side during the time when switch is on. During the interval when switch is off, the energy of magnetic inductor L_m charges C2 and C3 in parallel. Modes of Operation (Continuous Current mode of operation).

This section presents the operating principle of the proposed converter. In CCM operation, there are five operating modes as shown in Fig. 2 to 6 in one switching period. Fig. 7 shows typical waveforms

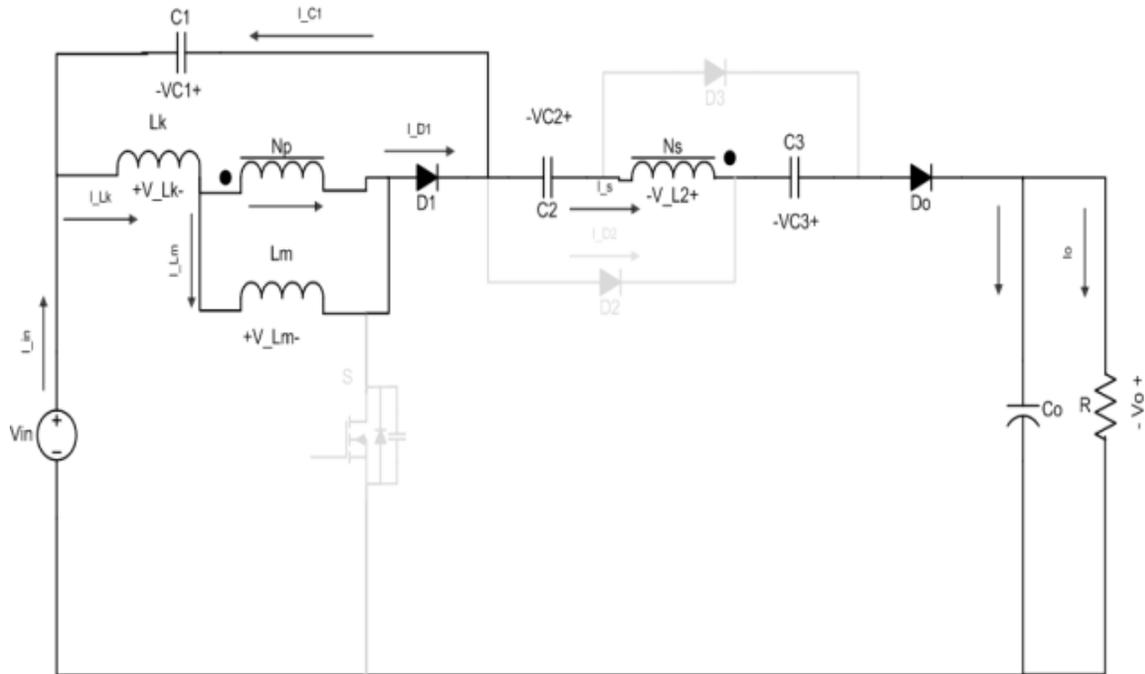


Fig. 5: Mode 4

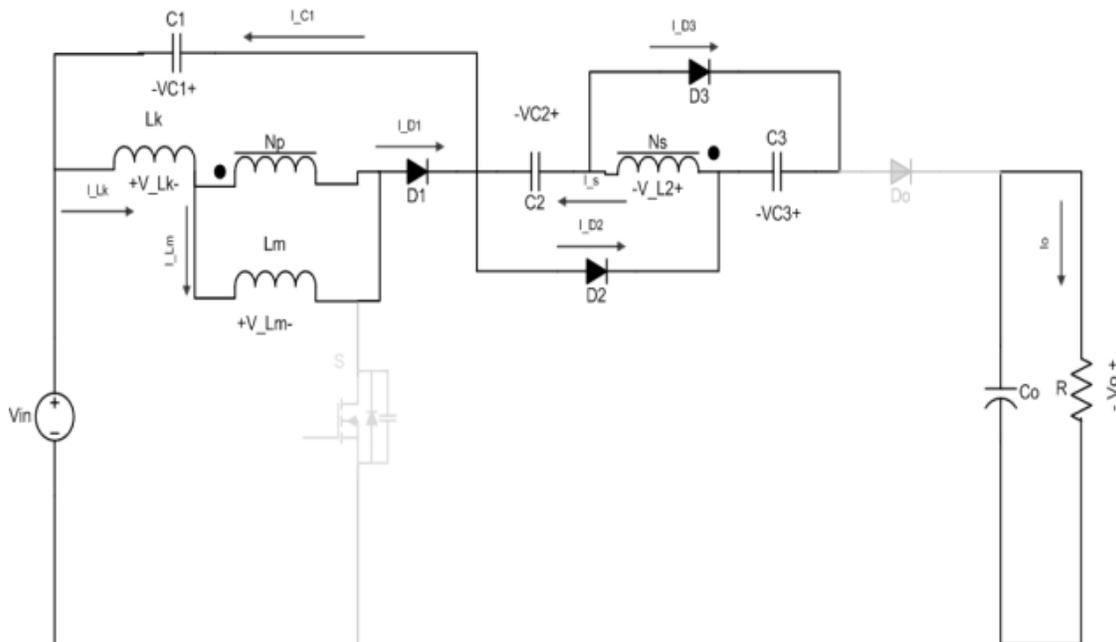


Fig. 6: Mode 5

Mode 1: Switch is turned on. Diodes D1, D0 are off, D2, D3 are on. The leakage inductor starts charging C1. Co discharges through R. Mode ends when D2 current becomes zero. This mode is of very short duration.

Mode 2: Switch remains on. D1, D2, D3 turned off. D0 is turned on. Energy from DC source is stored by the magnetizing inductor. This mode continues till the switch is off.

Mode 3: Switch remains turns off. Diodes D1, D2 and D3 remains turned off. D0 turns on. The parasitic capacitor of the switch is charged by the energies of leakage and magnetizing inductor. Co provides energy to load. Mode ends at the instant when D1 conducts.

Mode 4: Switch remains off. D1 and D0 are on and D2 and D3 are off. Leakage inductor energy is recycled.

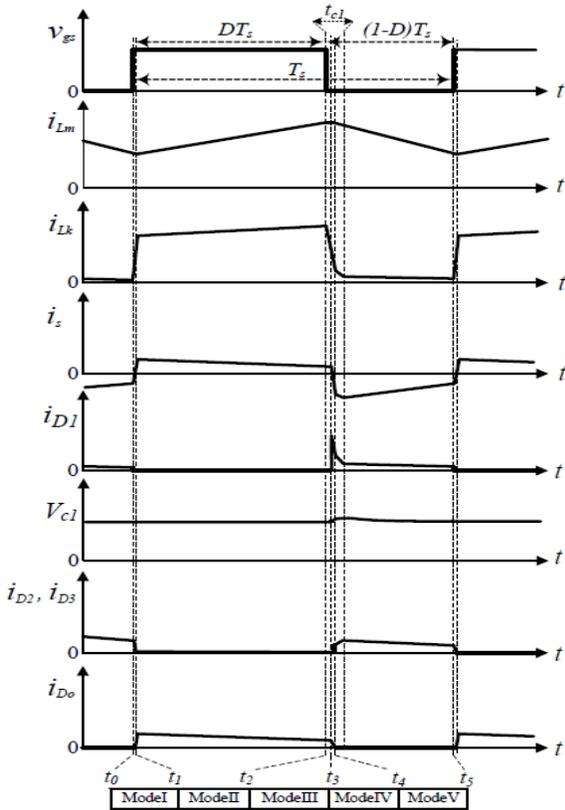


Fig. 7: Waveforms of the proposed converter

Coupled inductor continues charging Co and load. Mode ends when current through Do becomes zero.

Mode 5: Switch remains off. D1, D2 and D3 are on. Do is turned off. Leakage inductor Lk energy and magnetizing inductor Lm charge C1. C2 and C3 are charged in parallel. Mode ends when switch is turned on and cycle repeats.

STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

Modes 1 and 3 are very short and hence for steady state analysis only modes 2, 4 and 5 are considered.

The time for which capacitor C1 is charged by the leakage inductor energy:

$$t_c = \frac{2(1-D)T_s}{n+1}$$

Ts being the switching time:

$$k = \frac{L_m}{L_m + L_k}$$

$$n = N_s : N_p$$

Consider mode 2, by voltage division rule:

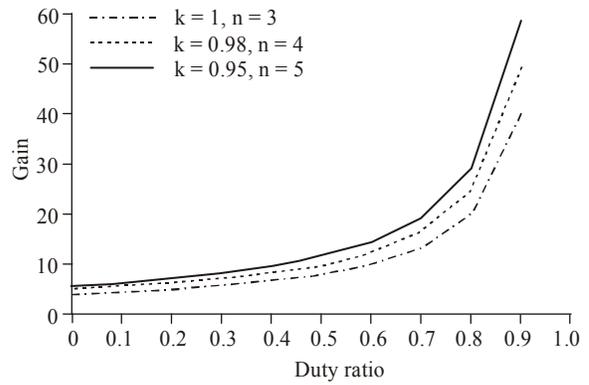


Fig. 8: Plot of gain and duty ratio for CCM

$$V_{Lk}^2 = \frac{L_k}{L_m + L_k} V_{in} = \left(1 - \frac{L_m}{L_m + L_k}\right) V_{in} = (1 - k) V_{in}$$

Across primary:

$$V_{L1}^2 = \frac{L_m}{L_m + L_k} V_{in} = k V_{in}$$

$$V_{L2}^2 = n V_{L1}^2 = nk V_{in}$$

By taking KVL:

$$V_o = V_{in} + V_{c1} + V_{c2} + V_{L2}^2 + V_{c3}$$

In mode 5, let the voltages across primary, secondary and leakage inductor be V_{L1}^5 , V_{L2}^5 and V_{Lk}^5 . Average voltage across inductor is zero. Therefore, for winding 1, 2 and leakage inductor:

$$\int_0^{DT_s} V_{Lk}^2 + \int_{DT_s}^{T_s} V_{Lk}^5 = 0$$

$$\int_0^{DT_s} V_{L1}^2 + \int_{DT_s}^{T_s} V_{L1}^5 = 0$$

$$\int_0^{DT_s} V_{L2}^2 + \int_{DT_s}^{T_s} V_{L2}^5 = 0$$

On solving:

$$V_{Lk}^5 = \frac{-D(n+1)(1-k)}{2(1-k)} V_{in}$$

$$V_{L1}^5 = \frac{-kD}{(1-D)} V_{in}$$

$$V_{L2}^5 = \frac{-knD}{(1-D)} V_{in}$$

Considering the capacitor voltages by KVL:

$$V_{c1} = -V_{Lk}^5 - V_{L1}^5 = \frac{D}{1-D} V_{in} \frac{(1+k)n+(1+k)}{2}$$

$$V_{c2} = V_{c3} = -V_{L2}^5 = \frac{nDk}{1-D} V_{in}$$

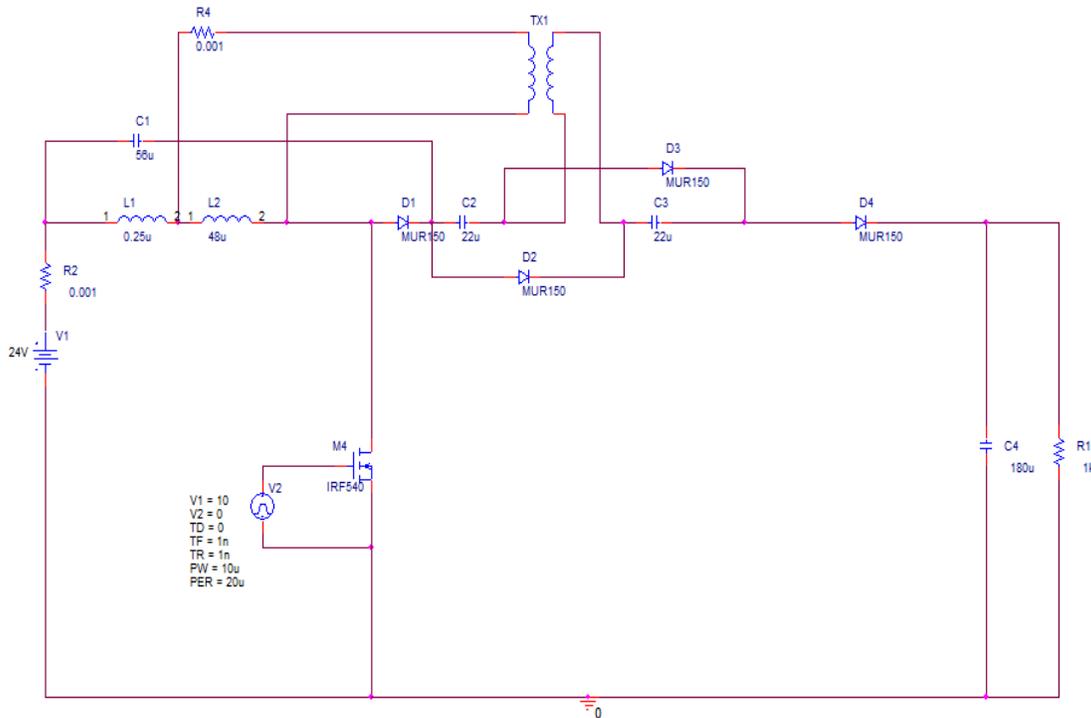


Fig. 9: Orcad schematic

By substituting the above values in the equation for V_o , Voltage gain:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{1+nk}{1-D} + \frac{D}{1-D} \frac{(k-1)+n(1+k)}{2}$$

Figure 8 shows the plot of gain versus duty ratio, we can infer that as duty ratio increases, the gain also increases exponentially for increase in turns ratio.

SIMULATION OF THE PROPOSED CONVERTER

The Proposed topology was simulated using PSPICE SOFTWARE with the following specifications:

Source voltage	24V dc
Switching frequency	50 kHz
Coupled inductor	$L_m = 48\mu\text{H}$, $L_k = 0.25 \mu\text{H}$ $N_p : N_s = 1 : 4$
Capacitors	$C_1 = 56 \mu\text{F}$, $C_2 = C_3 = 22 \mu\text{F}$ $C_o = 180\mu\text{F}$
MOSFET	IRF 540
Diode	MUR 150
Output voltage	333V dc

The proposed converter is simulated using PSPICE Software as shown in Fig. 9.

The output wave form is shown in Fig. 10. The input voltage of 24V is applied to the converter and the

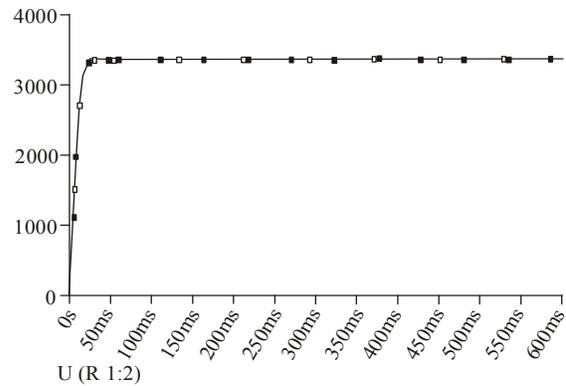


Fig. 10: Output voltage

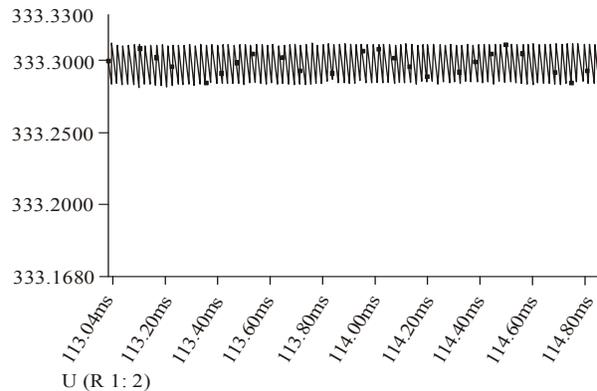


Fig. 11: Output voltage ripple

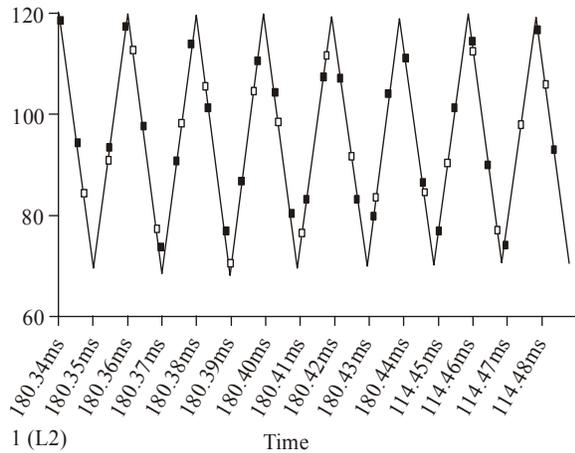


Fig. 12: Inductor current I(L2) showing CCM mode of operation

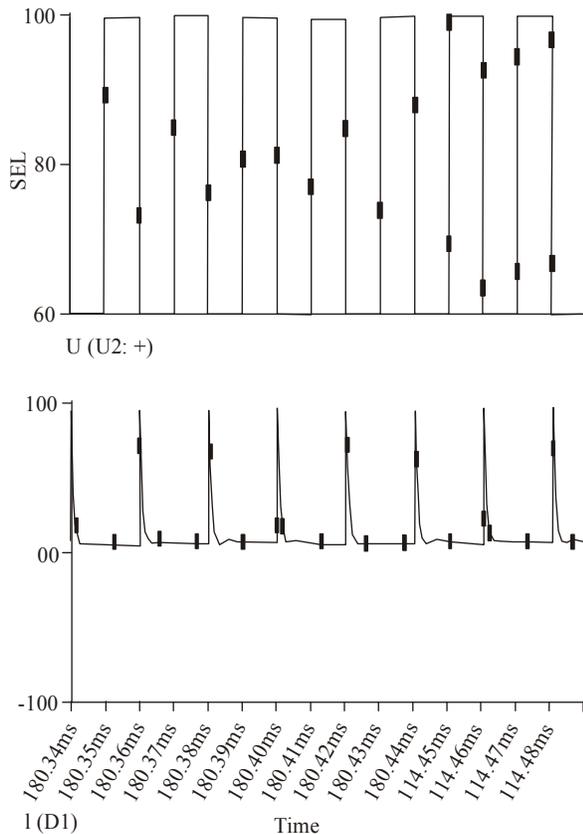


Fig. 13: Gate pulse and Diode (D1) current

output of 333V is obtained. The peak to peak ripple in the output is 0.02 V as shown in Fig.11.

Figure 12 shows the continuous current mode of operation of the converter with inductor current varying from 7-12 Amp. The Fig.13 shows gate pulses and the

current through diode D1 and it is clear that, soft switching is achieved and diode reverse recovery problem also alleviated.

CONCLUSION

A soft-switching dc-dc converter with high voltage gain for DG system has been proposed in this study. By using coupled inductor high gain was obtained. Using passive clamp circuit the leakage inductor energy was recycled. Hence reverse-recovery problem is alleviated. It provides a continuous input current and the ripple in the output voltage is also very low. The different modes of operation and steady state analysis were discussed. The setup was validated by simulation using Orcad software.

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