## **Research Article**

# Circuit Design Residue Logarithmic Number System (RLNS) Using the One-Hot System

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**Abstract:** In this study, we proposed high speed adder and low power and secure for module set  $\{2^{n}-1, 2^{n}, 2^{n}+1\}$  where we have provided to achieve maximum speed circuits for addition and subtraction computational method called the One-hot has been used where the delayed implementation using this method is that the size of a transistor in comparison with other previous implementations has improved dramatically. Another benefit of One-hot having a simple structure and regular implementation of the minimum power dissipation is the use of the Residue Logarithmic Number System arithmetic circuit with a balance can be very useful.

Keywords: Logarithmic number system, one-hot residue logarithmic number system, one-hot residue number system

## INTRODUCTION

Representation of numbers plays an important role in VLSI systems design. Considering high amount of mathematic operations in processors, there is a need for techniques that increase processing speed and decrease power consumption. One of designing methods for integrated circuit systems with high speed and low power consumption is application of One-hot coding. Using this method in a Residue Logarithmic Number System circuitry will be increases the speed and reduced power consumption.

Labafniya *et al.* (2010), has proposed a new circuits for one hot residue addition and subtraction using one barrel shifter structure. The proposed circuits have reduced amount of hardware and are able to generate the addition and subtraction results simultaneously.

Arnold (2005) has reported a new implementation of adders for the RLNS using combination of LNS and RNS to improve speed and memory efficiency and addition algorithm.

In Farshidi *et al.* (2010), new adders for modulo ( $r^{n}$ -1) with improvements power consumption are proposed. The authors have reached a significant reduction of applied transistors by scarifying the speed of the circuit and increasing the delay to 4 times the conventional OHR adders.

Hosseinzadeh *et al.* (2007) has proposed a novel design of an OHRNS-based adder circuit. This circuit has improved the number of transistors and power consumption. In this study, design of adder for

logarithmic residue number system used for fast arithmetic computation with general module set  $\{2^{n}-1, 2^{n}, 2^{n}+1\}$  for one hot coding are presented.

### NUMBER SYSTEM REPRESENTATION

**Residue Number System (RNS):** Residue Numbers System is a non-weight number system and one of its properties is limited distribution of carry numbers between modules in calculations. This system performs calculations on residue numbers simultaneously instead of a large number that considerably increases calculation speed and decreases power consumption. Residue Numbers System is used more in operators with repeated addition, subtraction and multiplies operations. Some of these applications include Digital Signals Processing, Digital Image Processing, Digital Filtering and etc. Application of this system causes increasing of calculation speed, decreasing of hardware circuit complexity and chip area and also good implementation of VLSI circuits (Burgess, 2003).

Residue Numbers System based on module sets is defined as  $m_i$ ,  $i = 1, 2 \dots n$  which relatively prime numbers, that is:

$$GCD(m_i, m_j) = 1 \quad , \quad i \neq j$$
<sup>(1)</sup>

And decimal value of x in non-weight system of residue numbers is shown as following:

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$$X = (x_1, x_2, ..., x_n), \qquad x_i = X \mod m_i$$
  
$$\exists q \Rightarrow X = q_i.m_i + x_i \qquad \text{where } i = 1, 2, ..., N \qquad (2)$$

where, x<sub>i</sub> obtains from remainder of division X by m<sub>i</sub>.

 $M = \prod_{i=1}^{n} m_i$  is dynamic range of this number in this system and x can be shown in this system as  $X = (x_1, x_2, ..., x_n)$  with the original form of that is a unique value for each integer and also  $\alpha$  in  $X \in [\alpha, M + \alpha)$  is a unique integer number (Taleshmekaeil and Mousavi, 2010; Jassbi *et al.*, 2010).

Calculation operation in Residue Numbers System classified in simple and difficult operations groups. Addition, subtraction and multiply are among simple operation group while sign detection and value comparison are among difficult operation group (Mousavi and Taleshmekaeil, 2010).

Simple operations in Residue Numbers System are as following:

$$X = (x_1, x_2, ..., x_n), \quad Y = (y_1, y_2, ..., y_n)$$
$$|X \cup Y|_M = \left( |x_1 \cup y_1|_{m_1}, |x_2 \cup y_2|_{m_2}, ..., |x_n \cup y_n|_{m_n} \right)$$
(3)

where, O can be addition, subtraction and multiply (Taleshmekaeil and Mousavi, 2010; Hosseinzadeh *et al.*, 2007).

Chinese Remainder Theorem (CRT) is used for transfer of Residue Numbers System to weight system. Chinese Residue System is defined as:

$$X = \left\langle \sum_{i=1}^{n} (x_i N_i)_{m_i} * M_i \right\rangle_{M}, \quad M = \prod_{i=1}^{n} m_i, \quad M_i = \frac{M}{m_i}$$
$$N_i = \left\langle M_i^{-1} \right\rangle_{m_i}, \quad i = 1, 2, ..., n$$
(4)

**Logarithmic Number System (LNS):** On the other hand Logarithmic Numbers System is considered as an efficient way for representation of numbers in VLSI processors. And major advantage of Logarithmic Numbers System is simple method of operations like multiply, division, root, power and sign detection that is taken from inherent characteristic of logarithm. On the other hand performing of operations such as addition, subtraction and shift to right and left be too difficult in this system. These characteristics make Logarithmic Numbers System appropriate for calculations that need not high accuracy and also operations that more ratio of multiply operations than divide operations (Arnold *et al.*, 2003; Lee and Burgess, 2003). In Logarithmic Numbers System, x number represents through x logarithm:

$$X \xrightarrow{LNS} \{s, x = \log_b(|X|)\}, \text{ s sign is} = \begin{cases} 0 & \text{if } X > 0\\ 1 & \text{if } X < 0 \end{cases}$$

b is logarithmic base of number x that in binary number systems equals two. Variables with capital letters in this system show the real values and corresponding variables with small letters are integers shown based on rules of Logarithmic Numbers System and Residue Numbers System. This rule and logarithmic properties lead to simplification of multiply, divide power and root operations. These operations in the system are as following:

Multiply: 
$$Z = XY = b^{x}b^{y} = b^{x+y}$$
,  $z = \log_{b} Z = x+y$   
Divide:  $Z = \frac{X}{Y} = \frac{b^{x}}{b^{y}} = b^{x-y}$ ,  $z = x-y$   
Root:  $Z = \sqrt[m]{X} = \sqrt[m]{b^{x}} = b^{\frac{x}{m}}$ ,  $z = \frac{x}{m}$ , m, ineger

Power: 
$$Z = X^m = \left(b^x\right)^m$$
,  $z = mx$ , m, ineger (6)

On the other hand in Logarithmic Numbers System, addition and subtraction operations become complicated and calculate as following:

$$\log_b(|X| + |Y|) = x + s_b(z)$$
  

$$\log_b(|X| - |Y||) = x + d_b(z)$$
(7)

where, z = y-x subtraction logarithm of operands. Addition functions of  $s_b(z)$  and subtraction functions of  $d_b(z)$  according to Gaussian addition logarithm are calculated as following:

$$s_b(z) = \log_b(1+b^z)$$
  
$$d_b(z) = \log_b(1-b^z)$$
 (8)

**Residue Logarithmic Number System (RLNS):** Combination of Logarithmic Number System and Residue Numbers System with mentioned characteristics can be useful. The rapid multiplication and division operations make this system suitable for applications with low accuracy and high operation capability. But these applications are dependent on simplicity of performed hardware, low power consumption, high speed of processing circuit operations (Arnold, 2005; Mousavi and Taleshmekaeil, 2010). In Residue Logarithmic Numbers System, x integer indicates through integer set of  $\{m_0, ..., m_n\}$ :

$$x_i = x \mod m_i \quad , i = 0, 1, \dots, n$$
<sup>(9)</sup>

where, the result of multiply calculation of  $Z_{mul} = X^*Y$ and divide calculations of  $Z_{div} = X/Y$  is as following:

for multiply: 
$$\hat{z}_i = (\hat{x}_i + \hat{y}_i) \mod m_i$$
  
for division:  $\hat{z}_i = (\hat{x}_i - \hat{y}_i) \mod m_i$   
 $q_s = x_s \oplus y_s$  (10)

where,  $q_s$  shows obtained sign and  $m_i$  equals selected module set in Residue Numbers System.

Addition operations in Logarithmic Residue Numbers System for two real values of X and Y and for production of T = X+Y by using the relation:

$$T = Y(1 + \frac{X}{Y}) = X + Y \tag{11}$$

Includes 3 steps:

- Division and obtaining Z, Z = X/Y.
- Obtaining W, W = 1+Z.
- Obtaining summation value of T, T = Y.W.

Corresponding values in Logarithmic Numbers System are shown by small letters of x, w, y, t and their real values are shown by capital letters of X, W, Y, T.

Divide operation for first step in Residue Logarithmic Numbers System is done through a subtraction integer circuit as following:

$$\widehat{z}_{i} = (\widehat{x}_{i} - \widehat{y}_{i}) \mod m_{i}$$
(12)

In the second step addition and subtraction functions of Logarithmic Residue Numbers System calculate as following:

$$w = \begin{cases} s_b(z) & \text{if } \mathbf{x}_s = \mathbf{y}_s \\ d_b(z) & \text{if } \mathbf{x}_s \neq \mathbf{y}_s \end{cases}$$
(13)

Table1: Decimal, binary and one hot residue module m<sub>i</sub>

| Decimal           | Binary | One-hot |  |
|-------------------|--------|---------|--|
| 0                 | 00000  | 10000   |  |
| 1                 | 00001  | 01000   |  |
| 2                 | 00010  | 00100   |  |
| •                 | •      | •       |  |
| •                 | •      | •       |  |
| • .               | •      | •       |  |
| m <sup>i</sup> -1 | 00001  | 00001   |  |

If w and x have any sign, positive and, then they have the same sign as z.

In the third step summation of Logarithmic Residue Number System calculates as following:

$$t_i = (\hat{y}_i + \hat{w}_i) \mod m_i \qquad \text{sign} = y_s \oplus w_s \tag{14}$$

**One-Hot Residue Number System (OHRNS):** One method of increasing the speed in the arithmetic operation, using the One-hot coding. We use for the representation number in the module mi of the m signals in the system when any moment only one signal is active and the rest of the signal is disabled and any active signals that indicate the remaining in the corresponding is module.

For the representation value number in this system, module remaining is from zero to  $m_i$ -1. Residue Numeral System circuit's implementation with One-hot having a regular structure are simple. Implementation of addition circuits remaining by the One-hot is done in rotating shifts (Hosseinzadeh *et al.*, 2007; Labafniya *et al.*, 2010). Representation number of decimal, binary and one hot residue module  $m_i$  is shown in Table 1.

**One-hot addition structure for mi module:** The input data structure (first data) as input value (second data) is shifted and the output is shown. This delay circuit is the size of a transistor Fig 1.

To operation addition such as the subtraction operation is just the input data (first data) the size of the shift value (data second) shift will be reverse (Jassbi *et al.*, 2007; Farshidi *et al.*, 2010).

Of problems in implementation this type of circuit with a One-hot for implement large module because the number of transistors in this structure rises to power. So for large module are not recommended. In order to module set  $\{2^{n}-1, 2^{n}, 2^{n}+1\}$  by putting value n = 2 to module set of  $\{3, 4, 5\}$  that reached to implement this system is appropriate.

**Proposed scheme for addition and subtraction in rlns:** Proposed circuit for addition and subtraction operations in Residue logarithmic number system a One-hot may include a separate form is provided.

**Direct transfer in module set \{2^{n}-1, 2^{n}, 2^{n}+1\}:** Direct transfer method in module set  $\{2^{n}-1, 2^{n}, 2^{n}+1\}$  for transfer of binary numbers system to Residue Numbers System is very simple and appropriate for efficient performance:

$$X = x_{3n-1}x_{3n-2}\dots x_{2n}x_{2n-1}\dots x_nx_{n-1}\dots x_0$$
(15)

Res. J. Appl. Sci. Eng. Technol., 5(1): 286-291, 2013

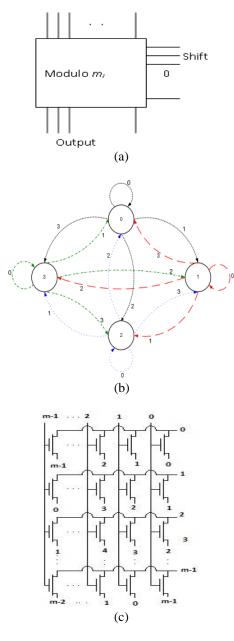


Fig. 1: a) Block diagram of the one hot adder b) Addition position for module four c) Internal structure of the One-hot adder circuit for a module of m<sub>i</sub>.

Binary number of x divides in to 3n bit parts of B1, B2 and B3:

$$B_{1} = \sum_{j=2n}^{3n-1} x_{j} 2^{j-2n}, B_{2} = \sum_{j=n}^{2n-1} x_{j} 2^{j-n}, B_{3} = \sum_{j=0}^{n-1} x_{j} 2^{j}$$
$$X = B_{1} 2^{2n} + B_{2} 2^{n} + B_{3}$$
(16)

Now we can obtain r<sub>i</sub> residue numbers as following:

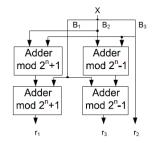


Fig. 2: Direct transfer circuit for module set  $\{2^{n}-1, 2^{n}, 2^{n}+1\}$ 

$$r_{1} = |B1 + B2 + B3|_{2^{n}+1},$$

$$r_{2} = B_{3}, r_{3} = |B1 + B2 + B3|_{2^{n}+1}$$
(17)

Direct transfer circuit for module set  $\{2^{n}-1, 2^{n}, 2^{n}+1\}$  is shown in Fig. 2.

Modified Chinese Remainder Theorem (MCRT): In Converters of R/B, we can use modified Chinese Remainder Theorem in which conventional CRT, M dynamic range for large scales, has less efficiency for performance. So we can use modified CRT with decreased module set which decrease dynamic range of M- $\prod_{i=1}^{i=n} m_i$  in conventional CRT in to dynamic range of M- $\prod_{i=2}^{i=n} m_i$  which in turn causes increasing of speed and efficiency and decreasing of power consumption:

$$X = x_{1} + p_{1} \left| \sum_{i=1}^{m} w_{i} x_{i}' \right|_{p_{2} \dots p_{m}}$$
  
where m >1, w<sub>1</sub> =  $\frac{N_{1} \left| N_{1}^{-1} \right|_{p_{1}}^{-1}}{p_{1}}$ , w<sub>i</sub> =  $\frac{N_{i}}{p_{1}}$ , for i = 2,3,..., m  
 $x_{1}' = x_{1}$ , and  $x_{1}' = \left| N_{i}^{-1} x_{i} \right|_{p_{i}}$ , for i = 2,3,..., m  
(18)

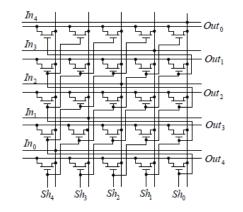


Fig. 3: Internal structure of the one-hot adder circuit for module 5

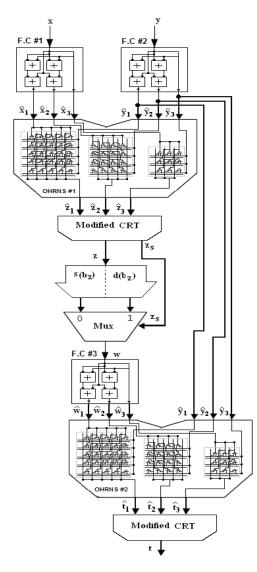


Fig. 4: Proposed hardware for addition and subtraction in RLNS

Addition circuit in logarithmic residue number system for module set of {2<sup>n</sup>-1, 2<sup>n</sup>, 2<sup>n</sup>+1}: After receiving integer numerical values of X and Y and by transferring them in logarithmic system representation with b base we can obtain x and y values. These values change in to  $(\hat{x}1, \hat{x}2, \hat{x}3)$  and  $(\hat{y}1, \hat{y}2, \hat{y}3)$  residues in module {2<sup>n</sup>-1, 2<sup>n</sup>, 2<sup>n</sup>+1} through direct transfer. Then  $(\hat{z}1, \hat{z}2, \hat{z}3)$  values calculate by using One-hot residue subtraction in mentioned module.

In this Part for subtraction of a One-hot should be a separate three circuit for the module by  $\{2^{n}-1, 2^{n}, 2^{n}+1\}$  implement that by putting value n = 2 to module set is  $\{3, 4, 5\}$ . Operations must subtract input data the size of the second shift will data reverse. Internal structure of the One-hot adder circuit for module 5 is shown in Fig. 3.

Using by modified Chinese Remainder Theorem change to logarithmic value of z and by calculating addition  $s_b(z)$  and subtraction  $d_b(z)$  function values in a parallel way we can obtain w. Addition or subtraction function is selected through z sign of bit. Next obtained values of  $(\hat{w}1, \hat{w}2, \hat{w}3)$  by direct transfer and by one-hot residue adder are summed with  $(\hat{y}1, \hat{y}2, \hat{y}3)$  and we obtain  $(\hat{t}1, \hat{t}2, \hat{t}3)$ . After obtaining the value of  $(\hat{t}1, \hat{t}2, \hat{t}3)$  through mentioned one-hot residue adder, finally, we can obtain t value by using modified Chinese Reminder Theorem.

But the use of techniques such as the CSA adder and subtract supplied by a parallel form can be useful but has a large overhead in delay and power consumption while the circuit delays in implementing the One-hot is a transistor. Results of the speed of your One-hot circuits are much faster and also because this circuit by changing two lines maximum input signal is changed as a result of the dissipation power is minimal.

This set of operations in the form of a simple hardware implementation, is presented in Fig. 4.

**Security:** Representation of used values in OHRLNS by one-hot coding for module are used as a bite encoded group with special order and calculation or processing operations are performed on these values in a coded manner and unauthorized hearer is not allowed to use it in one-hot coding is not aware of it, so he cannot use it at all.

Therefore in using OHRLNS is only sufficient to have a special module for having security in all intermediate and low levels and there is no need to increase number of used bits for encoding values.

#### **COMPARISON AND CONCLUSION**

Considering that the calculation of addition and subtraction in the Logarithmic Number System is difficult, many studies to increase speed and reduce power consumption in the system have been conducted.

In this study, we first Logarithmic Residue Number Systems and One-hot coding examined and logarithmic numbers to offer new system remains One-hot System spent.

Considering that One-hot Residue Number System having only one transistor delay in each operation is processing them so arithmetic operations will perform faster and because a signal is active only in its demonstration system, the minimum power consumption and also very simple and regular structure for the module set is optional. All this advantage makes the one-hot coding in the circuit implementation

#### Res. J. Appl. Sci. Eng. Technol., 5(1): 286-291, 2013

Table 2: Systems proposition compare numbers with previous designs

|        | Implementation structure | Delay   | Speed computations | Power consumption |
|--------|--------------------------|---|--------------------|-------------------|
| RLNS   | Usual                    | Greater (maximum value of bits selected module) | Usual              | Usual             |
| OHRLNS | Simple and regular       | Minimum (only one transistor)                   | Тор                | Minimum           |

Residue Logarithmic Number System that is creating a new system should be used. Table 2 Comparison between the One-hot Residue Logarithmic Number System with other numerical systems been shown that this system than other systems Numerical computing with fast and less power consumption than other systems is numerically And also has a regular structure and simple hardware circuits to implement it.

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