Research Article Low Power Narrow-Band Inductively Source Degenerated LNA in Presence of Substrate Noise

Pawan Kumar Singh and Sanjay Sharma ECED, Thapar University, Patiala, Punjab-147004

Abstract: This study presents the design and analysis of the inductively source degenerated low noise amplifier for the ultra-wideband application. This technique uses the linearization and the current MOSFET model for calculation of noise figure for the LNA. The impedance, two port network correlation matrix for the parasitic noise component and noise figure is also presented.

Keywords: Impedance matching, isolation, low noise amplifier, noise circles, noise figure, substrate noise

INTRODUCTION

Presently one of the most promising research interests is based on the radio receiver. Since the very first signal processing block of the radio receiver is low noise amplifier. The main purpose of the LNA is to amplify the received signal to the acceptable level with minimum self generated noise. The parameter of the LNA has significant impact on the sensitivity of the receiver. The gain, noise figure, nonlinearity and impedance matching are the most important parameter of the LNA design. The large signal must be accommodated by the low noise amplifier without distortion and present a specific impedance of 50Ω to the input source. The inductively source degeneration is having an advantage that inductor can potentially ease the difficulty in LNA design. The inductance value of the can be easily changed, this provides the flexibility in the tuning of the matching network (Heng et al., 2009; Chen et al., 2008). Many CMOS LNA have been reported in the recent year including distributed amplifier and resistive shunt feed-back amplifier. The prior design offers higher band width but larger power consumption which restricts its application (Chen et al., 2008). This study proposed the implementation of inductively source degenerated LNA. This inductor based LNA offers good performance in terms of noise figure and power consumption, but the use of inductor consumed more area on chip.

Two port noise representation: The noisy two ports can be represented in terms of noiseless two ports with corresponding two noise sources. Depending upon type of the noise sources many representation is been derived in Jung-Suk (2001) and is shown in Fig. 1. The impedance representation is for the series connection and the ABCD representation is for the parallel



Fig. 1: Two port representation of the noise source in (a) impedance representation (b) ABCD representation

connection in Fig. 1a and b. Each representation defines noise sources in term of correlation matrices mathematically (Jung-Suk, 2001).

The impedance representation is useful when the two networks connected in series, the correlation matrix will be:

$$\overrightarrow{C_{Z}} = \overrightarrow{C_{Z1}} + \overrightarrow{C_{Z2}}$$

$$\overrightarrow{C_{Z}} \triangleq \begin{bmatrix} C_{v1v1^{*}} & C_{v1v2^{*}} \\ C_{v2v1^{*}} & C_{v2v2^{*}} \end{bmatrix}$$

$$= 2kTR [\vec{Z}]$$
(1)

where, $\overrightarrow{C_Z}$ represents the correlation matrix of the impedance representation.

The ABCD representation is useful when two networks are cascaded:

$$\overrightarrow{C_{A}} = \overrightarrow{A_{1}} \overrightarrow{C_{A2}} + \overrightarrow{C_{A1}} \overrightarrow{C_{A}} \triangleq \begin{bmatrix} C_{vnvn^{*}} & C_{vnin^{*}} \\ C_{invn^{*}} & C_{inin^{*}} \end{bmatrix}$$
$$= 2kT \begin{bmatrix} R_{n} & \frac{F_{min-1}}{2} - R_{n}Y_{opt} \\ \frac{F_{min-1}}{2} - R_{n}Y_{opt} & R_{n}|Y_{opt}|^{2} \end{bmatrix}$$
(2)

Corresponding Author: Pawan Kumar Singh, ECED, Thapar University, Patiala, Punjab-147004

This work is licensed under a Creative Commons Attribution 4.0 International License (URL: http://creativecommons.org/licenses/by/4.0/).



Fig. 2: (a) Inductively source de-generated low noise amplifier and Simulation setup in ADS, (b) two port (small signal) representation of LNA

where, v_n , i_n are the noise equivalent voltage source and current source respectively and C_{vnin^*} is self power spectral density of the input referred noise. This representation is useful since the correlation matrix can be directly obtained from the noise characteristics (Jung-Suk, 2001; Chan *et al.*, 2010).

Low noise amplifier analysis: The schematic of inductively source degenerated low noise amplifier is given in Fig. 2a and b (Jung-Suk, 2001). The simulation is made in the Advance Design System (ADS. The impedance, noise figure and linearity are the most important parameters but this study is mainly focused on impedance and noise figure. The noise figure is first calculated using general two port theory and after this, noise figure is obtained using the general expression. The general two port ABCD representation is given in Fig. 1b.

$$F = 1 + \frac{\overline{|\iota_n + Y_s u_n|^2}}{\overline{\iota_s^2}}$$
(3)

where, F is noise figure, i_n is correlated with u_n and Y_s is source admittance.

$$=1+\frac{\overline{|(\iota_{n}+\iota_{u})+Y_{s}u_{n}|^{2}}}{\iota_{s}^{2}}$$
(4)

where: i_u is the component of i_n that is uncorrelated with u_n :

$$=1+\frac{\overline{|(Y_{c}\iota_{n}+\iota_{u})+Y_{s}u_{n}|^{2}}}{\overline{\iota_{s}^{2}}}$$
(5)

where, Y_c is correlation admittance:

$$= 1 + \frac{\overline{|u_u + (Y_c + Y_s)u_n|^2}}{\overline{u_s^2}}$$
(6)

$$= 1 + \frac{G_u + \left[(G_c + G_s)^2 + (B_c + B_s)^2 \right] \overline{u_n^2}}{\overline{u_s^2}}$$
(7)

This equation can be written as:

$$F = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s}$$
(8)

where, $\overline{u_s^2} = 4kT\Delta fG_s$, $\overline{u_u^2} = 4kT\Delta fG_u$, and $\overline{u_n^2} = 4kT\Delta fR_n$

To determine the minima of the noise figure, derivative of the equation is taken w.r.t. Y_s as:

$$\frac{\partial F}{\partial G_s} = \frac{-G_u - [G_c^2 - G_s^2 + (B_c + B_s)^2] R_n}{G_s^2}$$
(9)

$$\frac{\partial F}{\partial B_s} = \frac{2(B_c + B_s)R_n}{G_s} \tag{10}$$

$$\frac{\partial F}{\partial G_s} = 0 = G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \tag{11}$$

$$\frac{\partial F}{\partial B_s} = 0 = B_{opt} = -B_c \tag{12}$$

Using the Eq. (11) and (12) the Eq. (8) may be written as:

$$F = 1 + \frac{(G_{opt}^2 - G_c^2)R_n}{G_s} + \frac{\left[(G_c + G_{opt}) + (G_s - G_{opt})\right]^2 R_n}{G_s} + \frac{\left[(B_c + B_{opt}) + (B_s - B_{opt})\right]^2 R_n}{G_s}$$
(13)

Since from the Eq. (12) $B_c + B_{opt} = 0$, the Eq. (13) may write as:

$$F = 1 + 2R_n (G_{opt} + G_c) + \frac{\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2 \right] R_n}{G_s}$$
$$= F_{min} + \frac{\left| Y_s - Y_{opt} \right|^2 R_n}{G_s}$$

where,

$$F_{min} = 1 + 2R_n(G_{opt} + G_c)$$
(14)

The Eq. (14) is general expression for the minimum noise figure.

Considering the parasitic and digital substrate noise the G_{opt} and the R_n for the circuit given in Fig. 2b may be written as:

$$G_{opt} = \sqrt{\frac{\delta\omega^2 C_{gs}^2 (1-|c|^2) g_m^2 (1+\omega^2 \tau_b^2) 4kT}{5g_{d0} g_{mb}^2 S_{dsn}(f)}}$$
(15)

And when the parasitic and the substrate noise (digital substrate noise is modeled by a series resistance and an equivalent voltage source in parallel with the circuit as in Jung-Suk (2001) has been taken in to account then the R_n becomes:

$$R_n = \frac{4kT\gamma g_{d0} + g_{mb}^2 S_{dsn}(f) / (1 + \omega^2 \tau_b^2)}{4kTg_m^2}$$
(16)

From Eq. (12) = 0 and using the Eq. (15) and (16) in Eq. (14) the minimum noise figure for the LNA in the presence of digital substrate noise and considering the small signal parasitic is give as:

$$F_{min} = \frac{1 + 2\sqrt{\frac{4kT\gamma g_{d0} + g_{mb}^2 \frac{S_{sdn}(f)}{(1+\omega^2 \tau_b^2)} \delta\omega^2 c_{gs}^2 (1-|c|)^2}}{4kTg_m^2 \frac{5g_{d0}}{5g_{d0}}}$$
(17)

where, $S_{sdn}(f)$ is power spectral density of the digital substrate noise, g_m is transconductance, C_{gs} is gate to source capacitance g_{mb} and is the transconductance when the body bias effect is considered?

Impedance matching: The body bias effect and the gate-substrate capacitance are generally neglected and it is assumed that the transistor operates in the strong inversion in the analysis of the low noise amplifier. Considering these assumption analysis leads to the good results, but what will happen if the transistor is operating in moderate or weak inversion, in this case the gate-substrate capacitance (C_{gb}) and body bias effect must considered in the Fig. 2c:

$$V_{in} = i_{in} \left(j\omega L_g + j\omega L_s \right) + i_{in} \left(\frac{1}{j\omega C} \right) + i_0 j\omega L_s \qquad (18)$$

$$i_0 = g_m V_{gs} = g_m i_{in} \cdot \frac{1}{j\omega c_{gs}}$$
(19)

Substituting equation (19) in (18):

$$V_{in} = i_{in} \left[j\omega \left(L_s + L_g \right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \right]$$
(20)

$$Z_{in} = \frac{V_{in}}{i_{in}} = j\omega \left(L_g + L_s \right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}$$
(21)

And after considering the body bias effect and the gate-substrate (C_{gb}) capacitance, impedance after the stage can be approximated as:



Fig. 3: Layout generated in the ADS of Inductively source degenerated low noise amplifier

$$Z_1 = \frac{1}{\omega^2 L_s C_{gs} g_m} \cdot \frac{1}{1 + \frac{j \omega C_{gs}}{\omega^2 L_s g_m}}$$
(22)

And can be seen as the shunt of a resistor R with the capacitance C_{gs} and Z_{in} for this condition can be rewritten as:

$$Z_{in} = \frac{R}{1 + \omega^2 R^2 C^2} + j\omega \frac{\left[L_g - R^2 C \left(1 - \omega^2 L_g C\right)\right]}{1 + \omega^2 R^2 C^2} \quad (23)$$

where, R and C are given by:

$$R = \frac{1}{\omega^2 L_s C_{gs} g_m}$$
$$C = C_{gs} + C_{gb}$$

The proper choice of L_g and L_s can set the matching condition and L_g is used to set he resonance frequency. For the narrow band application the real part of the (23) will be equated to the source resistance and imaginary part will be zero. Using this assumption L_g and L_s can be approximated as:

$$L_s = \frac{R_s}{\omega_T} \cdot \frac{(C_{gs} + C_{gb})}{C_{gs}} \tag{24}$$

$$L_g = \frac{1}{\omega_0^2(c_{gs} + c_{gb})} \tag{25}$$

RESULTS AND DISCUSSION

The results are clearly depicting that the resonance frequency is 1GHz and the minimum noise figure is 1.5dB for the designed LNA. The values of the source inductor and the gate inductor to obtain the matching condition and at that particular condition the resonance frequency is defined.



Fig. 4: Comparison of Simulated S (1, 1) and S (2, 2) in for the presented LNA at different frequency of operation (solid lines for the ideal component and squares from Layout)



Fig. 5: Simulated isolation S (2, 1) in red for the presented LNA at different frequency of operation (solid lines for the ideal component and squares from Layout)



Fig. 6: Simulated minimum noise figure for the low noise amplifier at different frequency of operation (ideal for solid lines and square for the layout)

The comparison of simulated results obtained from the schematics and the layout in Fig. 3 is presented. S



1.0E6 1.0E7 1.0E6 1.0E7 1.

Fig. 7: Simulated noise figure in Smith chart at resonance frequency 1 GHz

Table 1: Low noise amplifier design parameter

Parameter	Values
L (Length)	0.35m
f_0 (Resonance Frequency)	1.0 GHz
<i>R_s</i> (Source Resistance)	50
V _{DD} (Supply Voltage)	2.4 V

Table 2: Low noise amplifier design results

Parameter	Values
L_q (Gate inductor)	7.5 nH
L_s (Source inductor)	2.6 nH
NF (Minimum)	1.5 dB

(1, 1) and S (2, 2) and the comparison with Layout results is shown in the Fig. 4, the resonance frequency for the designed LNA is seen and which is 1GHz. The isolation S (2, 1) is depicted in the Fig. 5 and the marker m3 showing that at 1GHz the isolation is 15dB. Figure 6 show the simulated noise figure andat resonance frequency the minimum noise figure is 1.5 dB and it can verify from the Fig. 7, the marker m1 is at 1GHz. From the Fig. 7 it is also noted that some of the noise circles will be disappeared when the frequency will be increased this is because the minimum noise figure will increase at increasing frequency and there cannot be circles corresponding the noise Fig. 7 the minimum noise figure. Table 1 and 2 show the LNA design parameters and the results.

CONCLUSION

The Low noise amplifier is designed for the narrow band application (0.5 to 3.5) GHz and the results are also validated by comparing with the results obtained from layout design in the presence of the digital substrate noise. The values of the source inductor and the gate inductor to obtain the matching condition are given and at that particular condition the resonance frequency is defined. The results are clearly depicting that the resonance frequency is 1GHz and the minimum noise figure is 1.5dB for the designed LNA. The values of the source inductor and the gate inductor to obtain the matching condition and at that particular condition the resonance frequency is defined.

REFERENCES

- Chen, W., G. Liu, B. Zdravko and A.M. Nikne Jad, 2008. A highly linear broadband CMOS LNA employing noise and distortion cancellation. IEEE J. Solid-State Circ., 43(5): 1164-1176.
- Chan, H.P., O. Yongho and R. Jae-Sung, 2010. Noise figure formulas of RF CMOS MOSFETs in the presence of digital substrate noise. IEEE Microwave Wirel. Compon. Lett., 20(11): 622-624.
- Heng, Z., F. Xiaohua and Edgar, 2009. Low power linearized ultra-wideband LNA design technique. IEEE J. Solid-State Circ., 44(2): 320-330.
- Jung-Suk, G., 2001. High frequency noise in CMOS low noise amplifiers. Ph.D. Thesis, Submitted to Stanford University.